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Shape Effects on the Performance of Si and Ge Nanowire FETs Based on Size Dependent Bandstructure

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1. Introduction

With the demand for high performance devices and packing density, scaling of Si based MOSFETs was aggressively driven into the nano-scale regime. In near future, however, conventional Si MOSFETs will be facing physical limitation [1]. Therefore, in order to overcome this challenge, search for other potential channel materials or device structures such as high carrier mobility materials and nanowires have been at the forefront of research during last decades. Among these different candidates, nanowire (NW) FETs have been explored to characterize the device performance experimentally and theoretically [2-5]. Although the most easily realisable and widely studied NW is circular Si NW as channel material, it was recently shown that triangular cross-section NW could also be fabricated [4]. This has opened up possibilities of characterizing device performance by changing channel cross-section. A theoretical study on this topic using the effective mass model or classical transport model has been carried out [5], but it lacks the detailed information of electronic structures in the nano-scale regime. These details actually hold the information on the key parameters which dominate the device performance.

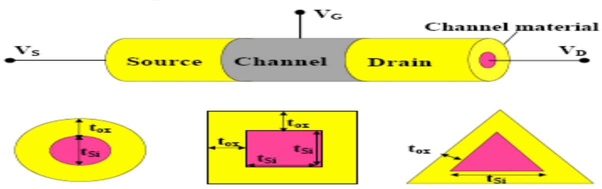

Fig. 1: A schematic of the simulated NW FETs with different channel cross section, namely circular, square and equilateral triangle.

In this work, we study the effects of the *shape, orientation* and *size* on ultimate performance of Si and Ge NW FETs, based on the full band calculations and ballistic transport for the fist time. A $sp^3d^5s^*$ tight-binding (TB) approach [6] is employed to investigate the electronic properties of Si and Ge NWs, where the device structure is shown in Fig. 1, in terms of E-k dispersion in order to accurately capture orientation as well as quantum effects in a nano scale system. Based on the calculated E-k dispersion, we engaged a semi-classical top-of-barrier MOSFET model [7] to evaluate the ballistic I-V characteristics of NW FETs in order to evaluate the ultimate performance of these semiconductor NW FETs with various effects. The effective insulator capacitance for various NW sizes and shapes are calculated using COMSOL (Fig. 2--left). We found that both shape and orientation affect the performance of Si and Ge NW MOSFETs through the gate capacitance and quantum effects. Moreover, their best performance configurations differ depending on the size.

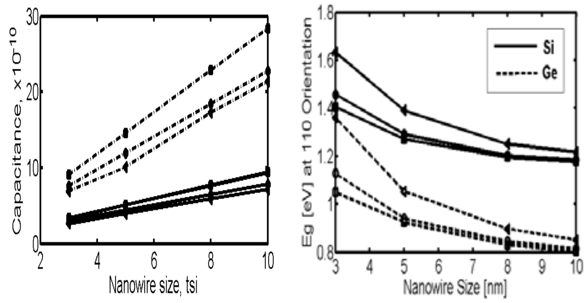

Fig. 2: (left) The insulator capacitance of NW with different size. Solid lines represent EOT=1.6nm while dotted lines represent aggressively scaled EOT=0.5nm. In both cases, square cross-section has the largest capacitance. Right: Energy bandgap (E_G) for <110> Si (solid lines) and <111> Ge (dotted lines) with different channel cross-section. The symbols resent the NW cross-section shape. The triangle shape NWs for both cases show the largest change in E_G.

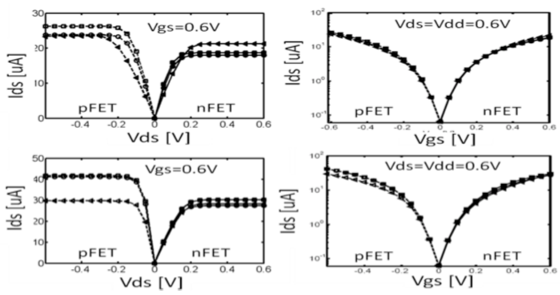

Fig. 3: (upper panel) transfer performance for 3nm Silicon NW MOSFETs with EOT=1.6nm for best orientation of different channel cross-section. The triangular cross-section (due to low effective mass) and square cross-section (due to high capacitance) NW provide best performance in nFETs and pFETs, respectively. (bottom panel) output and transfer performance for 3nm Ge NW MOSFETs with EOT=1.6nm for the best orientation of different channel cross-section. For both N-type and P-type MOSFETs, the square shape outperforms the other two types.

2. Results

Based on the bandstructure calculations, the variations of the bandgap energy at gamma point caused by the spatial quantum confinements are extracted, as shown in the right plot of Fig. 2. Next, performance of Si and Ge NW MOSFETs under different channel orientations and shapes are investigated based on their bandstructure. The best

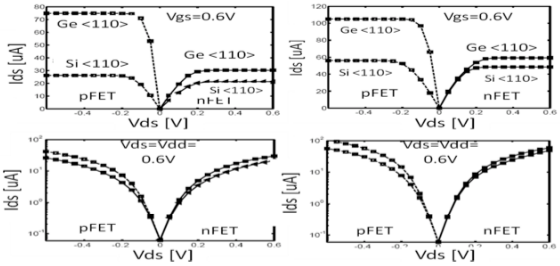

Fig . 4: Ids-Vds and Ids-Vgs comparison for best channel orientation and cross-section for 3nm Ge and Si NW with EOT=1.6nm(left panel) and EOT=0.5nm (right panel). The symbols are selected based on channel cross-section in all figures.

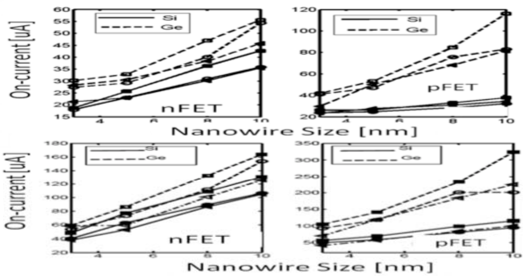

Fig. 5: On-current for best orientation with different channel cross-section for EOT=1.6nm (upper panel) and EOT=0.5nm (bottom panel). In general, square cross-section outperforms other cross-sections for Si and Ge. This is due to square cross-section having largest insulator capacitance.

performance configurations (in terms of orientation and shape) of Si and Ge NW FETs with the size of 3nm and EOT=1.6nm are selected in Fig. 3. For nFETs, the triangular shape, <110> Si and square shape, <110> Ge MOSFETs show the best performance. For pFETs, both Si and Ge MOSFETs show best performance along <110> with square shape cross-section. It can be attributed to the largest insulator capacitance offered by the square shape NW. However, in the Si nFET case, effective mass of triangular shape NW is much smaller than the others; therefore, its performance was enhanced. Next, we compare the performance of Si and Ge NW FETs under their best performance configurations with EOT=1.6nm and 0.5nm as shown in Fig. 4. Although Ge NW MOSFETs always outperform Si NW, the deviation in the case of EOT=0.5nm is smaller than the case of EOT=1.6nm. It is due to the quantum capacitance becoming small in the 1D system while the insulator capacitance increases as EOT decreases. When the insulator capacitance is comparable to the quantum capacitance, the latter starts to play an important role in the gate capacitance. When the quantum capacitance dominates the gate capacitance, the performance of the MOSFETs only depends on the number of degeneracy of Ek instead of effective mass [8]. The best performance of each case is summarized in Table. 1. Fig. 5 explores the channel cross-section effects for

			3nm	5nm	8nm	10nm
Silicon	N-type	CW	110	100	100	100
		RW	110	100	100	100
		TW	110	100	100	100
	P-type	CW	110	111	111	111
		RW	110	111	111	111
		TW	110	111	111	111
Germanium	N-type	CW	110	110	110	110
		RW	110	110	110	110
		TW	110	110	110	110
	P-type	CW	111	111	111	100
		RW	110	111	110	100
		TW	111	111	111	111

Table 1: Summary of best performance Orientation for different channel cross-section and NW sizes. Shaded cells represent best performance for each size.

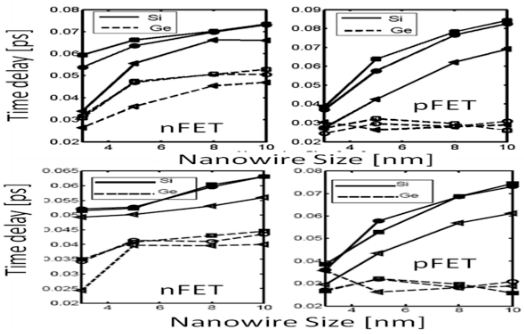

Fig. 6: Device intrinsic delay for best orientations with different channel cross-section and materials for EOT=1.6nm (up panel) and EOT=0.5nm (bottom panel). Ge has the smaller device intrinsic delay as compared to Si due to its effective mass being smaller than Si.

different NW size. For Si with NW sizes more than 5nm, square cross-section outperforms circular and triangular cross-sections. However, for Ge, square cross-section outperforms other cross-sections regardless of NW size. Fig. 6 shows the intrinsic device delay for best orientation of different channel cross-section NWs. As small delay is desired, triangular NW outperforms all other cross-sections. This could be explained from effective mass as time delay is directly proportional to effective mass and small effective mass will give small time delay.

3. Conclusions

We studied the shape and size effects of Si and Ge NW MOSFETs on device performance based on detailed full-band calculations and ballistic transport. A unique trend in these NW FETs is predicted due to a strong impact of quantum effects on effective mass caused by the various NW shapes and sizes. The square ones show the best performance in terms of highest ON-currents due to the largest insulator capacitance in square shape NW while the triangular cases shows the fastest intrinsic delay due to the smallest effective masses.

Acknowledgements

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