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Experimental investigation of electron-phonon scattering effect in strained Si nanowire FETs at low temperature

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1. Introduction

CMOS performance has been improved by the geometric scaling of the MOSFET structure to achieve high switching speed and low power consumption [1]. However, the scaling technology has become extremely expensive and complicated to gain the equivalent outcome. Since the transistor size has entered in a nano-scale regime, such improvements is no longer valid because of, 1) RC delay, 2) high leakage current due to the short channel effects and 3) threshold voltage shift due to the device size fluctuation. For further improvement, new structural alternatives are required, i.e., UTB, multi-gate, and nanowire [2]-[4]. From these alternatives, we have investigated on performance enhancement of Si nanowire transistors by introducing strain due to the peripheral thermal oxidation induced stress to the channel core [5], [6]. For further understanding of carrier transport mechanism in confined nano structure, electrical characteristics of the strained-nanowire FETs under low temperature are investigated to evaluate the influence of electron-phonon scattering in the device performance under low temperature.

2. Experiments

Si nanowire FETs are fabricated using SOI wafer, which consists 140nm of BOX layer, 45nm of active Si layer, and 15nm of cap-SiO_2 layer. Resistivity of the Si layer is 7~14Ω. Si nanowires are defined by EB lithography and dry etching. Nanowires are then oxidized at 850°C for 3h to introduce tensile stress in the wire core [6]. These nanowire devices are the back-gate controlled type, and all the electrical measurements are evaluated in accumulation mode. After the fabrication, we evaluated the electrical properties at temperature from 10K to 300K, with V_d=0.01V, V_s=0V, V_{bg}=0~37V, and voltage step of V_{bg_step}=0.1V. We also investigated the potential profile and electric field profile of the Si nanowires using three-dimensional (3D) device simulation.

3. Results and Discussions

Figure 1 shows the 3D device simulation results for the strained nanowire FETs (s-nwFETs); (a) potential profile and (b) electric field profile along the channel direction. For the both profiles, the device was evaluated at V_{bg}=10V and V_d=0.1V. The simulation results show that the potential and the electric field are uniform inside the nanowire. Note that the electric field is crowded at the bottom edge of the nanowire.

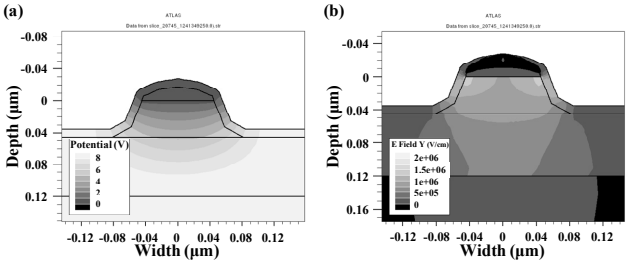

Fig.1 3D device simulation results; voltage biases are V_d=0.1V and V_{bg}=10V. Schematics of cross-sectional images of nanowire for (a) potential profile and (b) electric field profile. With progression from lighter color to darker color, the potential and electric field increase.

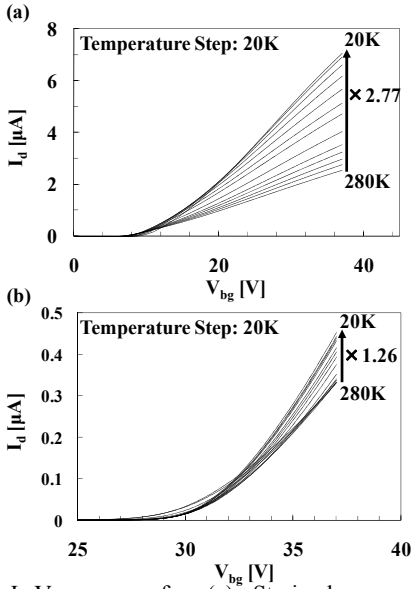

Fig.2 I_d-V_{bg} curve for (a) Strained nanowire FET of W=5000nm and (b) that of W=155nm. The electrical characteristics were measured at temperature range from 20K to 280K with the temperature step of 20K.

Figure 2 displays the I_d-V_{bg} characteristics of the fabricated s-nwFETs for (a) W=5000nm, and (b) W=155nm. Threshold voltage of W=155nm s-nwFET is at around 30V, and that of W=5000nm s-nwFET is at around 10V. This voltage shift is due to 1) reduction of the effective channel width caused by the oxidation of the side wall of nanowires, and 2) reduction of gate insulator capacitance (C_{OX}) due to

the increase in gate insulator thickness, that is caused by the oxidation from BOX layer. We confirmed that the improvement in drive current; 26% increased in W=155nm and 177% increased in W=5000nm by lowering the temperature of the measurement environment from 280K to 20K.

Transconductance (g_m) is defined by the following equation,

$$g_m \equiv \frac{W}{L_g}\frac{\varepsilon_i}{t_{OX}}\mu V_d \qquad (1)$$

where W is nanowire width, L_g is gate length, ε_i is insulator permittivity, t_{OX} is gate insulator thickness, μ is carrier mobility, and V_d is drain voltage. g_m is normalized by the structure factors. Since t_{OX} and W are variables, g_m is needed to be corrected as

$$g_m^* = g_m\left(\frac{t_{OX}}{W}\right) \qquad (2)$$

where g_m^* is the normalized transconductance.

Figure 3 (a) displays $g_{m\,MAX}^*$-T characteristics, where $g_{m\,MAX}^*$ is the maximum value of g_m^*. $g_{m\,MAX}^*$ is enhanced by a factor of 1.4 for W=155nm and 3.2 for W=5000nm, as temperature is lowered from 280K to 20K. This improvement in g_m^*, hence, the improvement in electron mobility, is due to suppression of reduction of electron-phonon scattering [8]. As lowering temperature, $g_{m\,MAX}^*$ of W=5000nm has strong dependence on temperature. While $g_{m\,MAX}^*$ of W=155nm shows weak dependence against temperature. CMOS performance can be enhanced by operating at low temperature, because of suppression of electron-phonon scattering at low temperatures [8]. Therefore, the enhancement in both devices with W=5000nm and W=155nm is attributed to the reduction of electron-phonon scattering. According to the previous research, average mean free path (MFP) of phonon in Si is estimated to be around 300nm [9]. The number of phonon mode is reduced, because the device size is much smaller than the MFP of Si at room temperature, resulting suppression of the electron-phonon scattering. This indicates that the devices smaller in size than MFP has discrepancy in mechanism of electron-phonon scattering compared to that for bulk. This also indicated that the influence of phonon depends on the device size, if the device size is smaller than MFP.

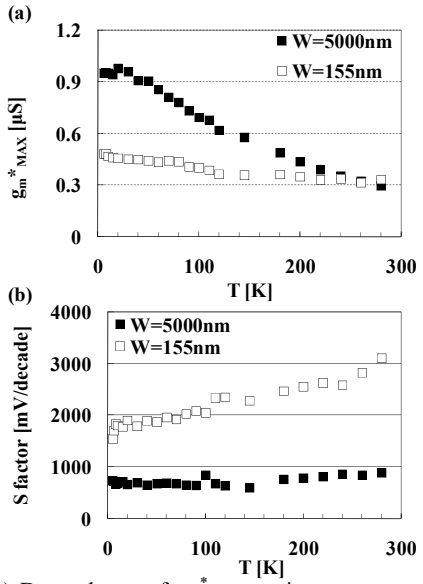

Fig.3 (a) Dependence of $g_{m\,MAX}^*$ against temperature for Si nanowire FET of W=5000nm and W=155nm. $g_{m\,MAX}^*$ increases by a factor of 3.2 for W=5000nm and 1.4 for W=155nm when temperature varies from 270K to 10K. (b) Subthreshold slope (S factor) against temperature for Si nanowire FET of W=5000nm and W=155nm. S factor decreases by 78% in W=5000nm, and 58% in W=155nm when temperature varies from 270K to 10K.

Figure 3 (b) shows the values of subthreshold slope (S factor) as a function of temperature. S factor are improved as temperature decreases. For example, S factor decreases 78% in W=5000nm s-nwFETs and 58% in W=155nm s-nwFETs as temperature decreases from 280K to 20K. This indicates that improved switching-off performance at low temperature can be achieved for strained nanowire FETs.

4. Conclusions

We evaluated the temperature dependence of normalized transconductance, g_m^*, the maximum value of g_m^*, and the subthreshold hold slope in s-nwFETs by evaluating I_d-V_{bg} at temperatures from 280K to 20K. As a result, g_m^* was enhanced by a factor of 1.4 for W=155nm and 3.2 for W=5000nm. S factor showed improved switching-off performance for s-nwFETs. This is due to the suppression of electron-phonon scattering at low temperature. The size effect in g_m enhancement indicates that the influence of electron-phonon interaction is different compared to that in bulk when the device size becomes smaller than MFP of phonon.

Acknowledgements

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References

[1] ITRS JEITA, 7 (2006)
[2] ITRS, 7, (2007)
[3] J. Y. Song et al, IEEE Trans. Nano-technol., vol. 5, pp. 186 (2006)
[4] M. Kobayashi et al, IEDM, 1007 - 1009 (2006)
[5] A. Seike et al, Appl. Phys. Lett. 91, 062108 (2007)
[6] A. Seike et al, Appl. Phys. Lett. 91, 202117 (2007)
[7] A. Seike et al, IEICE Tech. Rep., 108, 80, SDM2008-48, 35-39 (2008)
[8] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 287, Cambridge (2005)
[9] K. E. Yazdani et al, IEEE Proc. of Inter Society Conf. on Thermal Phenomena, 424 – 340 (2004)