Reducing the Gate Charge of Dual Gate Power VDMOSFET by Pseudo-Gate

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1. Introduction

Power Vertical Double-diffused MOSFETs (VDMOSFET) are widely-used on control switching, dc-dc converters, automotive electronics, and etc. High drive current, low gate charge (Q_G), low on-resistance (R_ON), high breakdown voltage (V_BR), and high inductive switching capability are the requirements in various fields [1,2]. In all these applications, low Q_G is the prime requirement to increase switching speed, which is governed by the poly-silicon gate area, especially the gate-drain overlapped region. One way is to shrink the gate length to reduce the gate-drain overlapped region. However, high R_ON will occur due to the parasitic junction FET (JFET) effect which arises from the adjacent wells. Consequently, a device figure of merit (F.O.M.) is defined as the product of R_ON × Q_GD for judgment for a specific V_BR[3].

To this end, Dual-Gate MOSFET (DGMOSFET) was proposed by removing partial gate-drain overlapped region [4]. Nevertheless, the DGMOSFET induces a high electric field at the end of the removed gate and sacrifices the V_BR and reliability issue. A thicker or a higher resistance epi-layer is used to maintain the V_BR, leading to a higher R_ON and higher conduction loss. Therefore, a floating p-region was added to eliminate the electric field concentration [5]. But it causes the rapid increase of R_ON. For this reason, a DGMOSFET with a npn-region was proposed to overcome it, which caused the unexpected result, a high electric field [6]. Furthermore, it needs additional masks and increases possible lithography misalignment during process.

Using a high dielectric (high-k) material to conduct electric field and induce electron have been proposed [7,8]. In this study, we propose a new DGMOSFET including a p-region and a silicon-nitride layer to carry out a low Q_GD device without complex process flow and overcome the problems mentioned above. The main features of the DGMOSFET are the reduced Q_GD by partial removed gate area and avoiding electric field crowding by the p-region. To compensate the removed gate region, a high-k material is used as pseudo-gate to conduct the electric field from the gate and attract the electron to invert the p-region.

2. Device Fabrication

The process begins with a arsenic-doped n-- epitaxial layer (Epi), which has a resistivity of 8 Ω·cm with a thickness of 18.5 μm for the specific V_BR over 250V, grown on top of silicon n+ substrate with (100) orientation. After field oxide (1 μm) was thermally grown, the active region and termination region were defined simultaneously. The gate oxide (0.07 μm), poly-silicon (0.55 μm) and pad oxide (0.1 μm) were formed and patterned, respectively, as the gate electrode. The well and source masks were used to define the p-well (5 × 10¹³ cm⁻²) and n-well (5 × 10¹⁵ cm⁻²), respectively. The DG structure and p-region (1.7 × 10¹² cm⁻²) were formed after n-well implantation by employing the same source masks. A silicon-nitride layer (or high-k material) was deposited as pseudo-gate to conduct the electrical field from the gate. In the process of the proposed structure, no additional masks are required. Here, we used a matrix mask to fabricate the conventional and proposed devices to prevent process vibrations. The gate length and the cell pitch of the conventional and proposed structure are 11 μm and 15 μm, respectively. The removed gate-drain overlapped length is 4 μm.

3. The Results and Discussion

Figs. 2 (a) and (b) show the measured gate charge curves of the conventional device and the proposed device, respectively. The Q_GD (Q_G) of the proposed device decreases from 29.6 nC (38.9 nC) to 19.2 nC (24.8 nC) at V GS = 10 V, respectively. It resulted from the gate-drain overlapped region was removed that led to the parasitic capacitance (oxide capacitance) was reduced. But, the
removed region will induce a high surface electric field and premature breakdown.

![Gate charge curves](image)

Fig. 2 The gate charge curves of the conventional (a) and the DGMOSFET with pseudo-gate (b). The devices were tested under the conditions of $V_{DD} = 200$ V and $I_D = 5.6$ A with the gate bias current ($I_G$) of 1 mA. $Q_G = I_G \times$ Time.

Hence a p-region was implanted to alleviate the high electric field but caused additional JFET effect and resulted in high $R_{ON}$. To lower it, a silicon-nitride layer (or high-k material), acts as a pseudo-gate, was deposited on the gate gap, which can deliver electric field from the gate to the p-region and attract the electrons to invert it. Tab. 1 summarizes the device characteristics. Though the slightly increased $R_{ON}$, from 387 mΩ to 452 mΩ, the reduction of F.O.M. of the DGMOSFET with the pseudo-gate is 24.2 % due to the lower $Q_{GD}$.

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<th>Conventional</th>
<th>Proposed</th>
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<tr>
<td>$Q_{GD}$ (nC)</td>
<td>29.6</td>
<td>19.2</td>
</tr>
<tr>
<td>$Q_G$ (nC)</td>
<td>38.9</td>
<td>24.8</td>
</tr>
<tr>
<td>$R_{ON}$ (mΩ)</td>
<td>387</td>
<td>452</td>
</tr>
<tr>
<td>F.O.M. (nC $\times$ mΩ)</td>
<td>11455.2</td>
<td>8678.4</td>
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Tab. 1 The characteristics of the conventional and the proposed structure. The $R_{ON}$ was tested by the Tektronix 371A under the conditions of $I_D = 6$ A and $V_{GS} = 10$ V.

Fig. 3 shows the simulated electric field intensity near the surface of the conventional, the device proposed in [5,6] and the proposed structure. The structure is much lower than the presented before but closes to the conventional. Lower electric field performance is beneficial to device reliability.

4. Conclusion

While the systems forward to high frequency, low $Q_G$ becomes more and more important because of high switching speed. In this study, we proposed the DGMOSFET with the pseudo-gate device to reduce the $Q_G$ and restrain the $R_{ON}$ comparing with proposed before. The improvement of the F.O.M. of the DGMOSFET with the pseudo-gate is 24.2 % comparing with conventional one. In addition, the electric field near the surface can be kept as low as possible.

5. References

[9] ISE TCAD Manuals, release 8.5