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Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp366-367

Liquid Phase Bonding Using Au Compliant Bumps for Fine-Pitch Solder Bump Interconnection

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1. Introduction

Three-dimensional (3D) chip-stacking technology has been extensively studied to meet the increasing requirements for highly-integrated low-power electronic circuits [1~3]. The interconnection which can provide high-density, large-number, and restriction-free-positioning electrical connections between chips plays a key role in this technology. We have proposed the concept of compliant bump to overcome most of problems of the conventional thermo-compression, i.e. non-melting bonding and to meet the requirements for 3D LSIs [4, 5]. Although the compliant bump technology offers non-melting bonding at relatively low compression force, when the bump number becomes several hundreds thousands to one million for a chip, it requires a large pressing load which cannot be generated as far as a conventional bonding machine is concerned.

To reduce the required pressing load for bonding, melt joining using solder bumps is attractive. The solder bump joining using existing bump technology is, however, hard to apply to high-density interconnection because the shrinkage of electrode pitch is restricted by electrical shorting between neighbors due to molten metal and the complex temperature/motion program limit the throughputs.

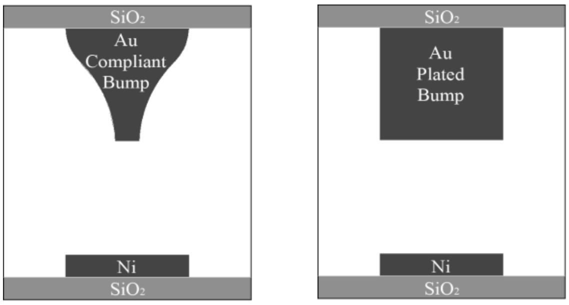
In this study, we propose a new interconnection bonding using the compliant bump and solder electrode. The shape of the compliant bump, which is typically a cone-like shape, allows molten solder to adhere to the surface and the spread of solder is constrained without complex temperature/motion program. Since the technology is a liquid-phase bonding process, the pressing load problem which mentioned above can also be overcome.

In this paper, we demonstrate the simulation and fabrication of this new interconnection technology. To carry out the simulation we experimentally determine the material parameters such as contact angle between molten micro-solder and electrode metals. Inter-chip connection with a pitch of 20 μm and an electrode size of 10 μm is demonstrated.

2. Modeling and Simulation

It is important to know how the shape of molten solder changes during the bonding. The direct observation of the behavior is hard to carry out. Instead we have tried to simulate the dynamic behavior of bonding and the resultant shape of electrode using a simulation software developed for fluid dynamics. The software we used was 'CoventorWare'. This software supplies a module to provide fluid dynamics analysis by finite elements method. In this study, we treat molten solder as fluid.

First, we need to build models and set molten solder's



(a) (b)

Fig. 1 Model of (a) compliant bump and (b) plated bump

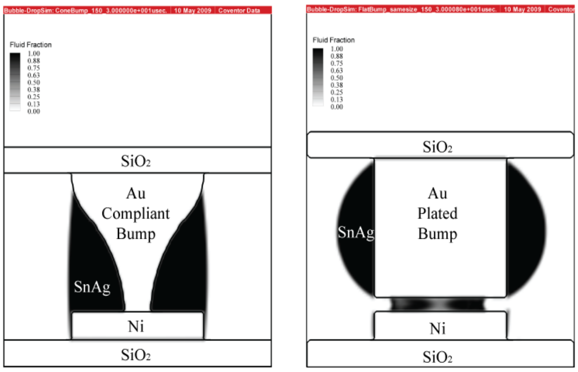
parameters. Figure 1 shows the models for cross section of the solid electrodes. Figures 1 (a) and 1 (b) are models for compliant bump and the conventional plated bump, respectively. The material for these bumps is Au. The material of the counter electrode, which corresponds to the so-called under bump metal (UBM) and passivation film are Ni and SiO_2, respectively. SnAg solder is set on the Ni UBM which is not shown in the figure.

To carry out simulation we need to know density and surface tension of SnAg and contact angle between SnAg and Au, SnAg and Ni, and SnAg and SiO_2. The density and surface tension of SnAg are provided by the literature [6,7] and listed in Table I. On the other hand, the contact angles were not available in the literatures. Therefore, we have measured the contact angles of SnAg to these three materials by observing with scanning electron microscope (SEM). The experimentally obtained values are also listed in Table I.

Table I Parameters for molten SnAg solder (523K)

Parameters	Data	Source
Density [g/cm^3]	7.0462	Literature[6~8]
Surface Tension [mN/m]	538.93	Literature[6~8]
Contact Angle [°]	SnAg - Ni: 15°	Experimentally obtained in this study
	SnAg – Au: 5°	
	SnAg – SiO_2: 143°	

Then the simulation was undertaken. It starts with bump and solder in initial position and ends up with bump into the molten solder. The result is shown in figure 2. We can see that the extent of molten solder adhered to the surface of bump. In the case of compliant bump, molten solder is constrained due to the cone shape. On the other hand, molten solder extends outside the bump area when the counter side is straight as like the plated bump. From this result, we can draw a conclusion that compliant bump is effective in minimizing the extent of the molten solder and, therefore, to produce fine-pitch interconnection.

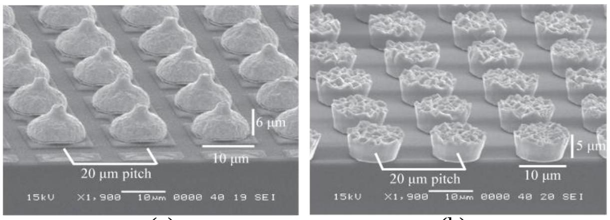


(a) (b)

Fig. 2 Simulation results of (a) compliant bump and (b) plated bump

3. Experimental Result

We carried out fabrication of bump and bonding test to verify the above simulation results. Both compliant bump and solder electrode was fabricated in sequence of UBM deposition, photolithography, and electro-plating. The cone-shaped hole to fill up with subsequent electroplating of Au and to form the cone bump was prepared by a novel process which enabled us to control the under-cut profile. The solder electrode was, on the other hand, fabricated using a conventional photolithography and electro-plating. Figure 3 shows the SEM image of compliant bump and solder electrode with a pitch of 20 μm and a diameter of 10 μm.



(a) (b)

Fig. 3 SEM image of (a) compliant bump and (b) solder electrode with 20 μm pitch and 10 μm diameter

The two test chips were flip-chip bonded under the conditions shown in table II. The compliant bump was set on upper side and solder electrode on the lower side.

Figures 4 (a) and 4 (b) show SEM cross-section view of the bump interconnection. We can see that the extent of molten solder is successfully restrained and the interconnection with 20 μm pitch is realized. Figure 4 (c) shows a simulation result after re-modeling the amount of solder.

Table II Bonding conditions

Number of bumps	12100 (110×110)
Pressing load	1.21 kgf (0.1 gf/bump)
Bonding temperature	250°C (Compliant bump)
	80°C (Solder electrode)
Bonding time	20 sec
Flux	OA5298HF4 provided by Cookson Electronics Co.

In terms of the consistency of the simulation and experiment, the shape is little different between them even after re-modeling. In the simulation, the compliant bump is all surrounded by molten solder (Fig.4 (c)). On the contrary, the solder does not climb up to the base (bottom) of the compliant bump in the experiment (Fig.4 (b)). A possible cause of the discrepancy between the experiment and simulation is the fact that the simulation does not take the intermetallic alloy formation into consideration. Further investigation is in progress to make the point clear.

4. Conclusion

In this study, we proposed a new interconnection for chip-stack and 3D integration using the compliant bump and solder electrode. The cone-like shape of the compliant bump minimizes the spread of the molten solder out of the Au-bump body area and, therefore, fine pitch interconnection can be realized. We demonstrated the flip-chip interconnection at 20 μm pitch. The motivation of our proposal was to achieve a large-number interconnection at a low pressing load which can be generated by a commercially available flip-chip bonder. In fact, we demonstrated the interconnection at the pressing load corresponding to 0.1 gf/bump, while over 0.5 gf/bump is required for thermo-compression bonding of Au bumps even when the compliant bump is employed.

Acknowledgements

This work is partially supported by Knowledge Based Cluster Project (2nd Term) of MEXT and the Grant-in-Aid for Scientific Research (No. 21246061) from JSPS.

References

[1] M.Koyanagi et al., IEEE Micro, **18** (1998) 17.

[2] K.Kameyama et al., *Extended Abstracts of SSDM* (2004) 276.

[3] C.A.Bower et al., *Proc. ECTC* (2006) 399.

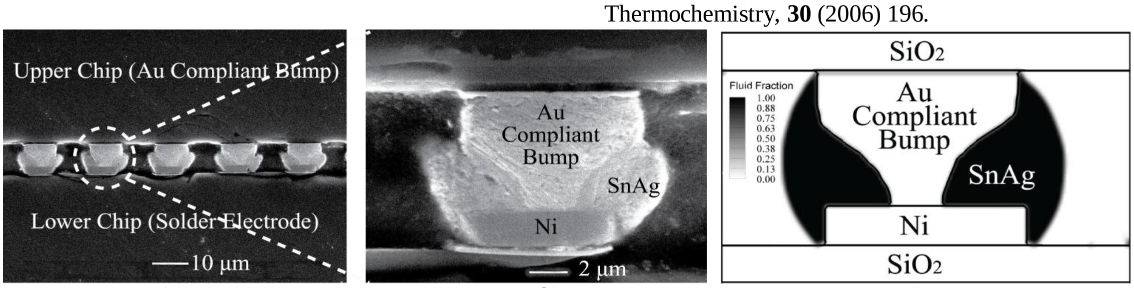
[4] N. Watanabe et al., *Tech. Dig. IEDM* (2005) 671.

[5] N. Watanabe et al., *Proc. ECTC* (2006) 125.

[6] Z. Moser et al., J. Phase Equilibria, **22** (2001) 254.

[7] M. Kucharski et al., Monatschefte für Chemie, **136** (2005) 1841

[8] R. Pajarre et al., Computer Coupling of Phase Diagrams and Thermochemistry, **30** (2006) 196.



(a) (b) (c)

Fig.4 (a) Cross section of an array of bump interconnection, (b) zoom view of a bump, and (c) a simulation result after re-modeling the compliant bump