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Evaluation of Thin LSI Wafers by Capacitance-Time (C-t) Measurement for the Process Characterization of Three-Dimensional (3D) Integration

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1. Introduction

Demands for the high-performance, high-speed, and highly integrated systems have been significantly increased for the future ubiquitous society. To meet the requirements, many researchers and product vendors recently present three-dimensional (3D) LSI technologies that can stack various kinds of functional blocks such as processor, memory, sensor, logic, analog and power ICs into one chip [1]. Through silicon via (TSV) formation and wafer bonding are well-known key technologies for the 3D LSI fabrication. In addition, wafer thinning is an indispensable process for 3D LSI. TSV size is an important factor to determine LSI performance, and therefore, high aspect ratio that is defined by the ratio of depth to width is required for TSV formation process. For the time being, when we employed TSVs with a width of 1 μm and 30-μm-thick wafers for 3D integration, TSV aspect ratio is assumed to be more than 30 μm.

Wafer thinning of less than 10 μm is technologically possible, however, the device performance of the thinned wafer would be seriously damaged by backside grinding and the following chemical mechanical polishing (CMP) due to their mechanical stress. Furthermore, the device performance of the thinned wafers would be also affected by the back end of line (BEOL) processes due to the metallic contamination even though the processes are proceeded at below 300 ºC. Therefore, the analysis of metallic contamination and device reliability for the 3D integration has been attracted much attention in recent years. However, the analysis such as knock-on effect by secondary ion mass spectrometry (SIMs) and Ar sputtering effect by X-ray photoelectron spectroscopy (XPS) has a great disadvantage in resolution. Capacitance-time (C-t) analysis and Zerbst method are highly sensitive and promising candidates for measuring very short generation lifetimes. This method can define the relaxation time of minority carrier in the depletion region, where ionized impurity are neutralized by minority carrier, and thereby, the depth of the depletion region is reduced [2,3].

In this paper, we investigate the generation lifetime and evaluate the metallic contamination by C-t method and Zerbst method using MOS capacitor fabricated on thinned silicon wafer with a thickness of 30 μm and without internal gettering layer.

2. Experimental

p-Type (100) silicon wafers with a thickness of 280 μm and a resistivity of 10-15 Ωcm were used for the crystallographic observation and MOS capacitor fabrication. The angle-(5°) polished silicon wafers were cleaved and then etched in $Hf+CrO_3(5M)+HNO_3+2g$ of $Cu(NO_3)_2$ in H_2O+HAc etchant for the observation of silicon crystal defects using optical microscope. To fabricate the MOS capacitor, 10-nm-thick thermal oxide were grown on the 2-inch wafers by thermal furnace at 900 °C under H_2 and O_2 ambience. After Al electrodes of 800 nm in thickness were formed by evaporation, the wafers were temporarily bonded to 100-μm-thick glass substrates. Then, thinning and CMP processes were performed until the thickness of the wafers decreased to 30 μm. After a 50-nm-thick Au as a metal impurity was evaporated on the back side of the thinned wafers, the wafers were annealed at 300 ºC in N_2 ambient for various annealing time. The fabrication process flows of the MOS capacitor formed on the 30-μm-thick silicon wafers are shown in Figure 1. The C-t measurement was performed using HP 4280A with 1-MHz oscillation signal at 10 mV.

3. Results and Discussion

Three-layer 3D chain pattern with copper TSV and micro-bump was previously fabricated and evaluated the EDS mapping images, as shown in Fig. 2. Si atoms, which include the oxide and silicon substrate, are clearly shown in Fig 2 (b). However, metal of copper and Al atoms are not clearly observed as shown in Figs. 2 (c) and (d). It is difficult to determine the metal contamination and device reliability. From these results, the interconnection between TSV and micro-bump, between bump to Al wire, it shows clearly. However, to determine the defects of silicon crystal and metallic contamination is difficult. Therefore, to observe the crystal defects in the angle-(5°) polished Silicon wafers, the samples were cleaved and etched in wright etchant. Figure 3 shows the representative low angle-(5°) polished silicon wafers of micro defects within the silicon wafer, and illustrated a defect before and after etched low angle-(5°) of a silicon wafer. When increased etching time, it shows to represent defects like as dark spots near the bottom side of silicon [4]. The enlarged FE-SEM images show the defects after wright etching. When increased the etching time, defect number is increased. But the shape of defect does not change. It is considered that the defect shape is related the Si substrate orientation (100) and the increased defect number are due to the depth etching with a very high anisotropy wet etchant. From these optical microscopy observations, the defects, which called an internal gettering (IG) layer, exist near the bottom side of silicon where places on ~140μm from top side of silicon. On the other hand, the top side of silicon surface and near the region does not have any defects, which called a denuded zone. From those results, for the process characterization and for analyzing the performance of MOS capacitor of the 30μm thickness of silicon wafer without IG layer, the C-t method is introduced. Figure 4 shows the measured C-t plots of MOS capacitor on the thinned wafer. The Al electrode is circular with $\phi = 500\mu m$ and gate oxide thickness is 10nm. Substrate is *p*-type wafer with $N_d=1.0\times10^{15}/cm^3$. The evaluation is performed using the Zerbst plots. The Zerbst plot are the growth of the inversion charge Q_{inv}, which is proportional to the time derivative $-d(C_{ox}/C)^2/dt$, is drawn as a function of $C_f/C-1$, which is the normalized effective depth as shown in Fig. 5, where the C_{ox} is the oxide capacitance, C_f is inversion capacitance and measured C is the high frequency capacitance, respectively. Generation lifetime of MOS capacitor on the 30μm thickness of silicon wafer as a function of various annealing time at 300 °C are shown in Fig. 6. While the Au diffused with annealing at 300 °C for 15min, the lifetime is significantly decreased. When the annealing time is 15min, 30min, 40min, 60min and 120min at 300 °C for the Au diffusion, the generation lifetime is 175μs, 39μs, 37μs, 32μs and 25μs, respectively. It means that a few Au atom reach the $Si\text{-}SiO_2$ interface while the initial annealing at 300 °C for 15min.

4. Conclusions

In summary, the study of the IG layer and denuded zone is clearly observed using wright etching and optical microscopy observation. Furthermore, MOS capacitors on the 30μm thickness

wafer without IG layer were fabricated and evaluated using C-t and Zerbst method. As the results, the MOS capacitor on the wafer of 30μm thickness without IG layer is significantly affected by metallic contamination. As the results, it is confirmed that C-t method and Zerbst evaluation method is suitable for the 3D process characterization and for analyzing the performance of 3D semiconductor device of the under 30μm thickness of silicon wafer.

References

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Acknowledment

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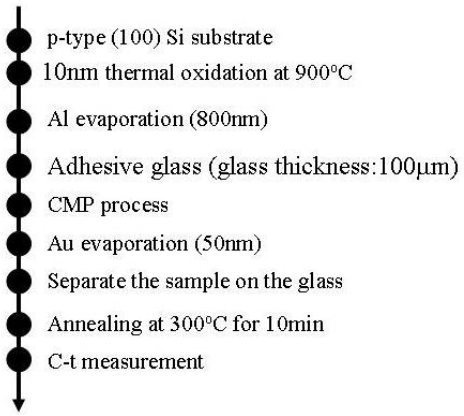

Figure 1 Process flows for the fabrication of MOS capacitors on 30-μm-thick silicon wafers.

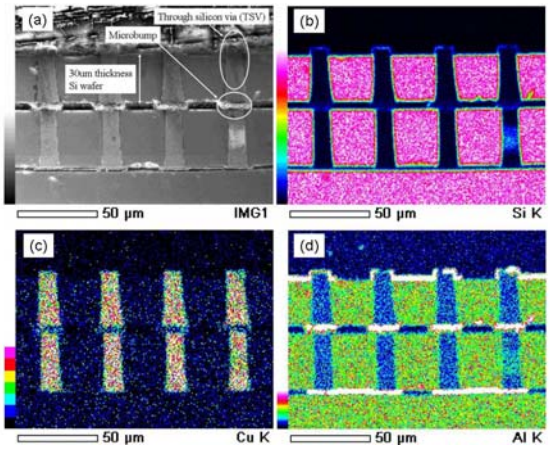

Figure 2 FE-SEM and EDS mapping images of 3D chain pattern with Copper TSV and micro-bumps: cross-sectional view of FE-SEM image (a), and mapping image of Si (b), Cu (c), and Al (d) atoms.

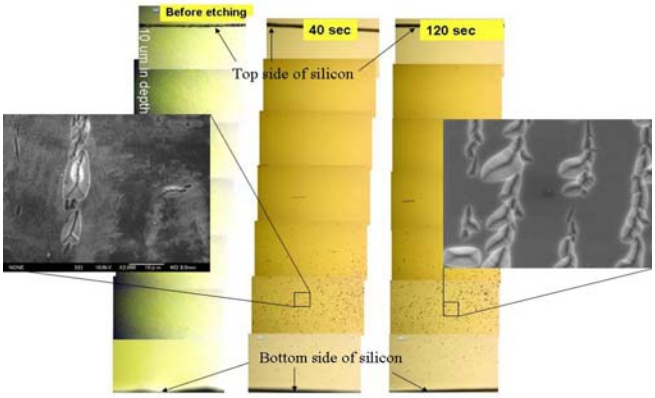

Figure 3 Top view of optical photomicrograph of micro defects and denuded zone within angle-(5°) polished silicon wafers (the enlarged FE-SEM images show the defects after wright etching).

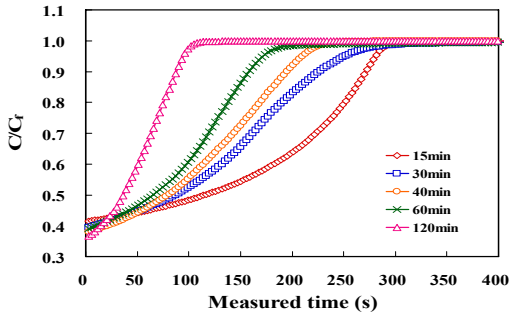

Figure 4 Measured C-t plots of the fabricated MOS capacitor on the 30-μm-thick thinned silicon wafer without IG layer.

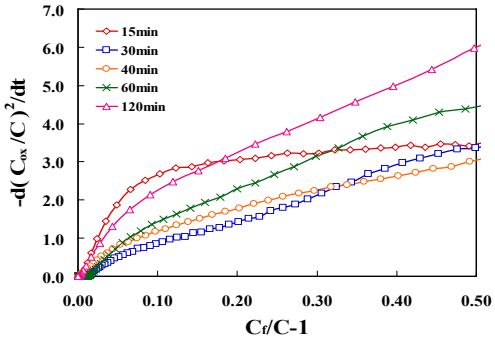

Figure 5 Time derivative $-d(C_{ox}/C)^2/dt$ as a function of $C_f/C-1$ (Zerbst plot).

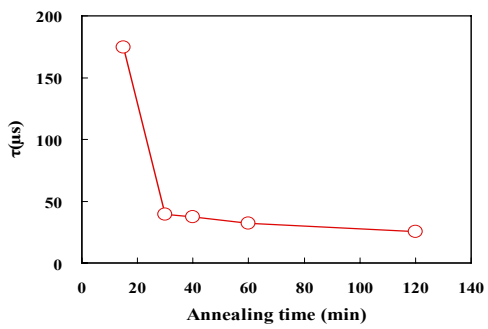

Figure 6 Generation lifetime of MOS capacitor on the 30-μm-thick silicon wafer without IG layer as a function of annealing time.