Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp378-379

Suppression of V_{th} Variability for n-MOSFET in Dual Oxide Formation Process

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1. Introduction

It is widely known that the variability of MOS transistor characteristics becomes worse as the design rule shrinks [1]. However, it has been understood that the variability of MOS transistor characteristics becomes worse even relative large size transistor when the process condition relate to the gate oxide and polysilicon is inappropriate. The pre-clean condition before gate oxidation affects the variability of threshold voltage(V_{th}) of transistor seriously. This variability caused by pre-clean condition could be suppressed by optimizing dopant concentration of gate polysilicon .

2. Experiment

The evaluation samples were prepared by dual gate oxide CMOS process. The oxide thicknesses of thinner and thicker oxides are 7 and 10nm, respectively. The experimental splits were set to pre-clean condition of 2nd gate oxidation and gate polysilicon condition. Fig. 1 shows the process flow and the splits are shown in table I. In the dual oxide process, pre-clean before 2nd gate oxidation is delicate, since 1st gate oxide exists partially on the wafer. So, standard pre-clean sequence, like RCA-cleaning, could not be used. So, the pre-clean before 2nd gate oxidation is performed without HF and APM. In this study, we used 2-type wet-station as split condition. One is dip-type, another is spray-type. Wafer is soused in cleaning fluid at dip-type, and sprayed with cleaning fluid at spray-type. Both machine dispose cleaning fluid (SPM) in every batch. As the gate polysilicon condition, we used 2-type polysilicon. One is doped-poly Si, another is undoped-poly Si. Doped-poly Si is formed by LP-CVD at 550°C 70nm with phosphorus concentration $3.0\times10^{20}cm^{-3}$. Undoped-poly Si is formed by LP-CVD at 620°C 70nm, then implant phosphorus $2.5\times10^{15}cm^{-2}$ or $4.0\times10^{15}cm^{-2}$ for undoped-poly Si case. The polysilicon is annealed 900°C in N_2 ambient for 30min and deposited 100nm WSix by CVD.

We used the large-scale variability evaluation test circuit developed by Tohoku University. The test circuit can measure a large-scale number of transistor-parameters in a short period of time. It is very suitable for statistical variability analysis [2][3]. There are more than 1.2milion transistors per chip with variation of dimensions and structures. In this study, we focused on V_{th} of W/L=1.5/0.4μm thinner gate oxide NMOS-transistor. Transistor array of this dimension has 64K transistors per chip.

3. Results and Discussion

The V_{th} distribution of 64K W/L=1.5/0.4μm size NMOS transistor is shown in Figs. 2(a), (b), and Figs. 3(a), (b).

Figs.2(a) and (b) show the V_{th} distribution of pre-cleaning dependence at same gate polysilicon condition. Fig.2 (a) shows undoped-poly Si gate case. It is observed pre-clean dependence. The standard deviation of V_{th} spray-type is 0.018V. This value is very high and hard circuit design. On the other hand, Fig. 2(b) shows undoped-poly Si gate case. The standard deviation of V_{th} is very close in each splits and value is low, without pre-clean dependence.

Figs 3(a) and (b) show the V_{th} distribution comparison of the gate polysilicon dependence at same pre-clean condition. Fig. 3(a) is dip-type case. The V_{th} distribution is very close and the value is low, without polysilicon dependence. Fig. 3(b) is spray-type case. The standard deviation of V_{th} is smaller than that of doped-poly Si, and lower phosphorus concentration undoped-poly Si shows lower V_{th} variability.

Fig. 4 shows the V_{th} variability of each split. The variability for combination of doped-poly Si and spray-type is the worst of all. Moreover, the variability of undoped-poly Si depends of doping concentration, and the variability of decreases with a decrease of doping concentration. This result suggests that the combination of pre-cleaning and gate polysilicon condition affects to the transistor variability.

To understand this phenomenon, MOS capacitor analysis was done. Fig. 5 shows the CV curves of each split. Undoped-poly Si($3.6\times10^{20}cm^{-3}$) split shows smaller capacitance in inversion region compares to other splits. This is caused by gate polysilicon depletion. The phosphorus concentration near SiO_2/gate-poly interface of doped-poly Si is higher than any other undoped-poly Si split.

The gate oxide breakdown characteristics are shown in Fig. 6. There is no failure mode in all splits and they indicate intrinsic breakdown voltage. This means the gate oxide quality is almost the same in each split.

Fig. 7 shows V_{th} variability as visible image. Each dot corresponds to each transistor. Each array has 64K transistors. The contrast of each dot means difference from average V_{th} of array. Bright dot means higher V_{th}, dark dot means lower V_{th}. Fig. 8 shows close-up of Fig. 7.

Split1 (spray-type pre-clean and doped-poly Si) image is rough compare to other split images. But global uniformity over array seems same at every split. It suggests V_{th} variability between neighboring transistors is large at split1.

Process difference between split1 and split3 is only pre-clean. V_{th} variability is caused by pre-clean. The root cause of V_{th} variability is gate oxide variability in local area. It seems that phenomenon is brought by no uniform chemical oxide under pre-clean. Spray-type pre-clean makes no uniform chemical oxide. But split4 and split5, V_{th} variability is suppressed even though using spray-type pre-clean. This effect is brought by gate depletion. Lightly gate depletion diminishes influence of local variability chemical oxide.

The variability can be suppressed by optimizing the pre-gate clean and dopant concentration in poly Si/gate oxide interface. These results are very useful to form a high performance and quality devices with dual oxides. Through the discussion above, we found out key process to suppress V_{th} variability. The pre-clean condition of 2nd gage oxidation in dual oxide device is one of important processes.

3. Conclusions

The chemical oxide formed at pre-clean should be homogeneous thickness. Dip type is better than spray type to achieve uniform chemical oxide. Dopant concentration of gate polysilicon is also important. Mild depletion of gate polysilicon is effective to disable the influence of chemical

oxide variability. In this study, we used *W*/*L*=1.5/0.4μm size MOS transistor. This size seems large enough today. V_{th} variability gets worse even relative such large size MOS transistor, if the treatment of gate electrode formation steps is inappropriate.

Acknowledgements

Concerning this study, I would like to express great thank to Tohoku University member - Dr. Miyamoto, Mr.Watabe, Mr. Fujisawa, and Mr. Kumagai - cooperated in the evaluation, discussion and suggestion.

References

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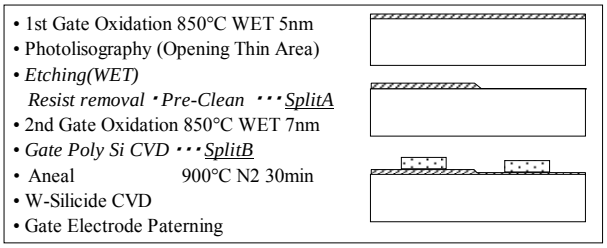

Fig.1 Process Flow

Table I Split Table

1). It is a wet scrubber from which fresh SPM is always supplied.

	Split1	Split2	Split3	Split4	Split5
Pre-Clean [1]	Spray-type	Dip-type	Dip-type	Spray-type	Spray-type
Poly Si CVD	Doped ($3\times10^{20}cm^{-3}$)	Undoped	Doped ($3\times10^{20}cm^{-3}$)	Undoped	Undoped
Poly I/I	-	$2.5\times10^{15}cm^{-2}$ ($3.6\times10^{20}cm^{-3}$)	-	$2.5\times10^{15}cm^{-2}$ ($3.6\times10^{20}cm^{-3}$)	$4.0\times10^{15}cm^{-2}$ ($5.7\times10^{20}cm^{-3}$)

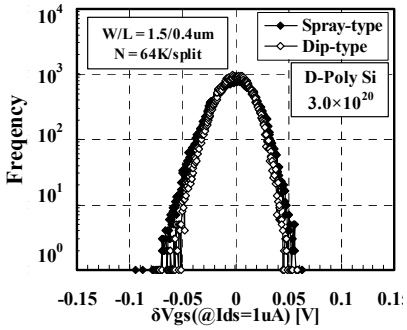

Fig. 2(a) The V_{th} distributions of the pre-clean splits. The V_{th} variation of Spray-type split is larger than that of Dip-type.

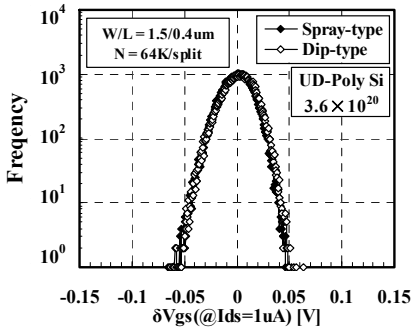

Fig. 2(b) The V_{th} distributions of the pre-clean splits. Spray-type and Dip-type.V_{th} variability is the same.

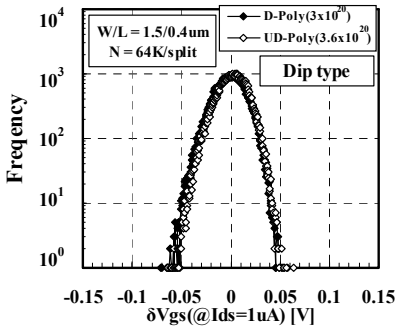

Fig. 3(a) The V_{th} distributions of the poly Si splits. The V_{th} variation doesn't have of each splits.

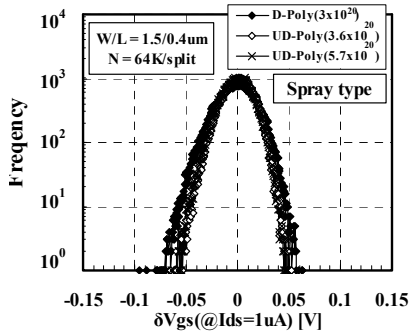

Fig. 3(b) The V_{th} distributions of the poly Si splits. The V_{th} variation of D-poly Si split is larger than that of UD-poly Si.

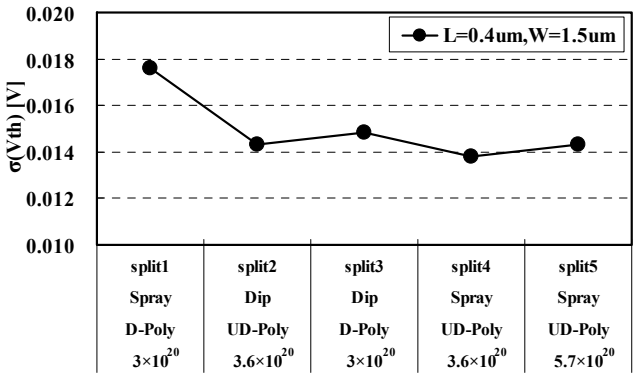

Fig. 4 V_{th} variation of each splits. V_{th} variation of Split1 is the largest.

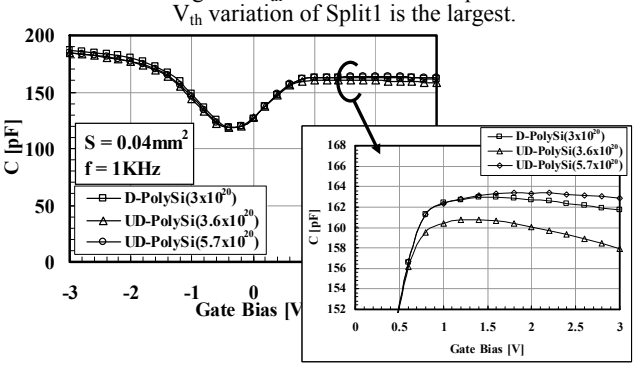

Fig. 5 C-V Curves of each Splits. Capacitance in the state of accumulation is smaller than D-poly($3\times10^{20}cm^{-3}$) split and UDope Poly($5.7\times10^{20}cm^{-3}$) split, UDope Poly($3.6\times10^{20}cm^{-3}$) split is made depletion.

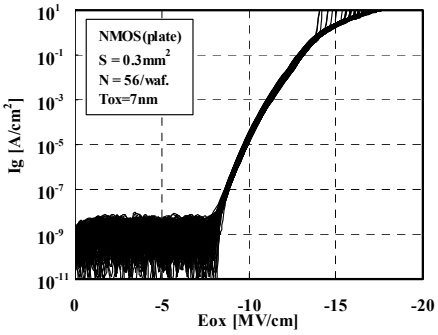

Fig. 6 Oxide breakdown voltage IV curve. A-mode and B-mode defective is not appeared in all splits.

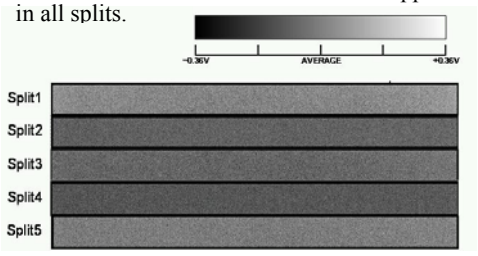

Fig. 7 Results of V_{th} variability making of visible. It is shown from the black to white by 4096 steps, and the V_{th}-value is clearly understood.

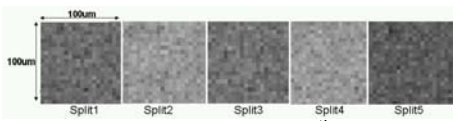

Fig. 8 The close-up of $100um^2$ area. . 1 square means 1 Transistor. The contrast is different between the adjoining transistors in split1.