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New Observations of FN Stress Induced Performance Degradation of RF MOSFETs

Bingjun Xiao[1], Lijie Zhang[1] , Ru Huang[1*], Dake Wu[1], Liangliang Zhang[1], Fei Song[1] and YangYuan Wang[1]
[1]Institute of Microelectronics, Peking University, Beijing 100871, China, Email: ruhuang@pku.edu.cn
Phone: 86-10-62757761, Fax: 86-10-62757761, *E-mail: ruhuang@pku.edu.cn

1. Introduction

Continued shrinking of RF MOSFET gate length leads to thinner silicon oxide film and higher electrical field and thus can results in reliability issues [1]. Previous works to evaluate the RF circuit degradation mainly focused on hot carrier instability (HCI). HCI stress will induce interface states and oxide traps near the drain junction and thus causes the degradation of f_t and f_{max} of MOSFETs and circuit failure [2-4].

However, the reliability issue of RF MOSFETs under FN stress which often occurs in some applications, such as RF switcher and passive mixer, has rarely been reported. In these circuits, the drain of the MOSFETs is biased at low voltage and the effect of HCI stress is considerably reduced, and meanwhile MOSFETs mainly suffer a uniform stress in the oxide film, which means FN stress becomes the dominant factor for the degradation of these circuits. The degradation of RF MOSFETs under FN stress is expected to exhibit different characteristics from that under HCI stress due to different physical mechanisms.

In this paper, the impacts of FN stress on the RF performance of 130nm MOSFETs are investigated. It is first reported that f_t and f_{max} shows different degradation tendency under FN stress. In addition, the gate bias exerts converse influence on the trapped charge generation during stress and the trapped charge impact on the performance degradation induced by FN stress. The optimized gate bias can be obtained when considering the tradeoff between the dependence of RF performance on the gate bias and the generation rate of trapped charges during stress, which can give valuable design guidelines for RF CMOS circuits.

2. Experiments

The MOSFET devices with multi-fingers were fabricated using 130nm SMIC technology with W/L=2.5μm/0.13μm and finger number N_f=64. The thickness of the gate oxide was about 2.5nm. Ground-Signal-Ground (GSG) test structure was used for both DC and RF characterization, as illustrated in Fig. 1. Agilent 4155C was used for DC biasing and current-voltage (I-V) characteristic measurement. S-parameters were measured up to 10GHz using a HP8150 Network Analyzer. On wafer open-short de-embedding was done and the gain of current and power is extracted. Then f_t and f_{max} are extrapolated in the plot of gain versus frequency. Small-signal modeling parameters are extracted from Y-parameters according to the sub-circuit model of RF MOSFETs as shown in Table 1.

For FN stress study, the gate voltage was stressed at +3.5V for nMOSFET and -3.5V for pMOSFET, unless otherwise specified. The stress was interrupted when the various transistor parameters were measured. This stress-measuring cycle was repeated until oxide breakdown.

3. Results and Discussion

Fig. 2 gives the comparison of the degradation between nMOSFET and pMOSFET. It can be observed that pMOSFET shows severer degradation than nMOSFET. As a result, the FN reliability of pMOSFET is more important and only the degradation of pMOSFET is further studied in this work.

Fig. 4 gives the shift of S-parameters before and after FN stress for 1000s. The gate DC bias voltage for S-parameter measurement is -0.6V and the drain voltage is set at -1.2V. It can be seen that all S-parameters changed after FN stress. Small-signal modeling parameters are extracted from Y parameters and the comparison between the degradation of RF performance under FN stress and HCI stress [7] is given in Table 2.

As shown in Table 2, unlike the degradation caused by HCI stress, C_{gd} decreases after FN stress. The difference is probably due to the fact that FN stress does not induce so many interface traps as HCI stress does [9], which can also be proved by the little degradation of subthreshold slope as shown in Fig. 3. The decrease of C_{gd} is probably due to the trapped charge in the oxide induced by FN stress. These charges will screen the electrical field lines from the gate and reduce the surface potential near the drain region and thus result in the decrease of C_{gd}. On the other hand, the reason why C_{gs} does not show the same degradation behavior is probably that a strong inversion layer already existed near the source region and the surface potential near the source region is less susceptible to the influence of the trapped charges.

Fig. 5 shows the degradation of f_t measured at different gate voltages. It can be observed that the higher the gate voltage, the lower the f_t degradation compared with the fresh device. This can be explained by lower reduction of g_m and higher reduction of C_{gd} at this gate voltage (Fig. 6). In addition to the density of inversion carriers, g_m at relatively higher gate voltage is also controlled by the surface mobility degradation which is influenced by the effective vertical electrical field. Since the effective vertical field can be weakened due to the trapped charges induced by FN stress, surface scattering can be reduced for less mobility degradation. Thus the decrease of g_m at higher gate voltage due to FN stress is smaller in spite of the carrier density decreasing.

Since f_t measured at higher gate voltage shows lower reduction after the same FN stress and on the other hand MOSFETs stressed under higher gate voltage will suffer faster degradation, there is an optimal operating gate voltage for MOSFETs which can make tradeoff between the dependence of RF performance on the gate bias and the rate of trapped charge generation. Assuming that the criterion for lifetime of RF MOSFETs is the degradation of f_t to 15GHz [8], the lifetime of RF MOSFETs is extrapolated from their stress voltage to their operating voltage, as shown in Fig.7. The optimal gate voltage for the longest lifetime is found to be -0.78V in this work, where the overdrive voltage is -0.42V.

The f_{max} is another important figure of merit. It is interesting to find that f_{max} measured at gate voltage higher than -0.7V will increase after FN stress (Fig. 8), which indicates that the degradation of f_{max} will not be a major issue when it is biased at a gate voltage higher than this operating point. The increase of f_{max} at high measuring gate voltage may be ascribed to the decrease of C_{gd} and thus the increase of power conversion efficiency at the input in spite of the decrease of current gain and f_t. Since higher gate voltage will induce more power consumption and accelerate the generation of trapped charge, -0.7V is considered as the best gate operating voltage in this work, where the overdrive voltage is -0.35V and the decrease of C_{gd} can exactly compensate the impact of current gain and f_t degradation on power gain and f_{max}.

4. Conclusions

The impacts of FN stress on the RF performance of MOSFETs have been extensively investigated in this work. It is found that pMOSFET shows more severe degradation than nMOSFET. Both f_t and f_{max} with the gate voltage of -0.6V decreased considerably after FN stress. The gate bias exerts different influence on the trapped charge generation during stress and trapped charge impact on the performance degradation induced by FN stress. The optimized gate bias is obtained considering the tradeoff between the dependence of RF performance on the gate bias and the generation rate of trapped charges. It is also found that f_{max} measured at the gate voltage higher than certain value even increases after FN stress and the optimal condition is then given.

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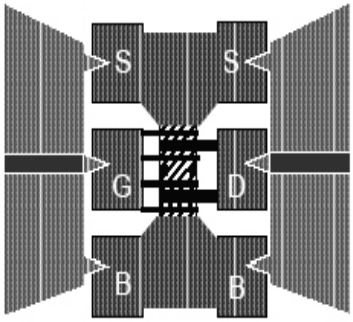

Fig. 1 The test structure of RF characterization in this work.

$$(1)\quad C_{gg}=\frac{\mathrm{Im}(Y_{11})}{\omega}$$

$$(2)\quad C_{gd}=-\frac{\mathrm{Im}(Y_{12})}{\omega}$$

$$(3)\quad C_{gs}=\frac{\mathrm{Im}(Y_{11})+\mathrm{Im}(Y_{12})}{\omega}$$

$$(4)\quad C_{ds}=\frac{\mathrm{Im}(Y_{22})+\mathrm{Im}(Y_{12})}{\omega}$$

$$(5)\quad R_g=-\frac{\mathrm{Im}(Y_{21})+\omega C_{gd}}{\omega g_m C_{gg}}$$

$$(6)\quad R_{ds}=\frac{1}{\mathrm{Re}(Y_{22})}\qquad (7)\quad g_m=\mathrm{Mag}(Y_{11}+Y_{12})$$

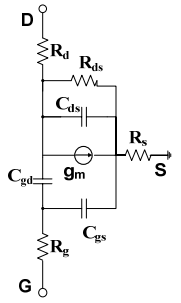

Table. 1 The modeling parameters extraction according to the sub-circuit model of RF MOSFETs.

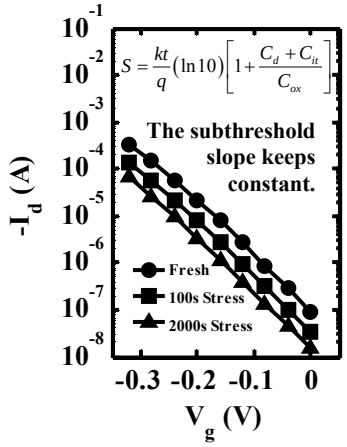

Fig. 3 The subthreshold current of MOSFET before and after stress. The subthreshold slope keeps constant, which indicates that FN stress induces fewer interface traps.

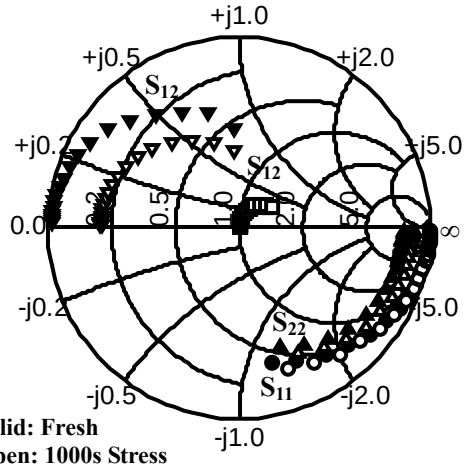

Fig. 4 Typical results of S parameter degradation of pMOSFET after FN stress.

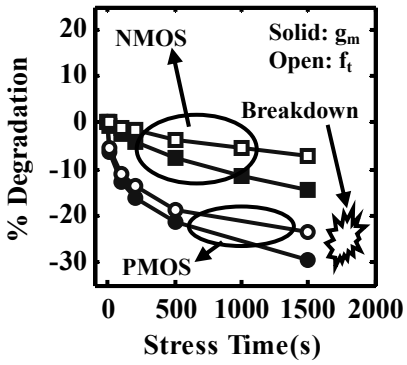

Fig. 2 The g_m and f_t degradation of nMOSFET and pMOSFET stressed @ V_g= +3.5V for nMOSFET and -3.5V for pMOSFET. It can be found that pMOSFET shows severer degradation.

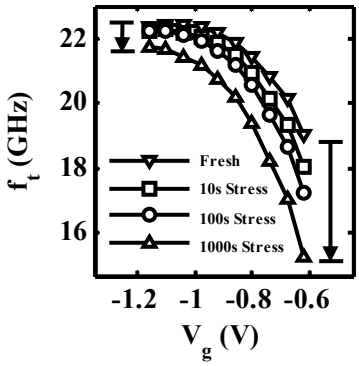

Fig. 5 The dependence of f_t degradation on the measuring condition under FN stress. The higher the gate voltage, the lower f_t degradation.

[7]	C_{gs} (pF)	C_{gd} (pF)	C_{ds} (pF)	R_g (Ω)	R_{ds} (Ω)
Fresh	0.215	0.0574	0.38	1.7	75
After HCI Stress for 15000s	0.239	0.0578	0.38	1.7	76.2

This work	C_{gs} (pF)	C_{gd} (pF)	C_{ds} (pF)	R_g (Ω)	R_{ds} (Ω)
Fresh	0.1367	0.0553	0.1211	14.1871	233.9143
After FN Stress for 1000s	0.1436	0.0522	0.1215	13.3214	373.7312

Table. 2 The comparison of small-signal model parameters after HCI stress [7] and FN stress (this work).

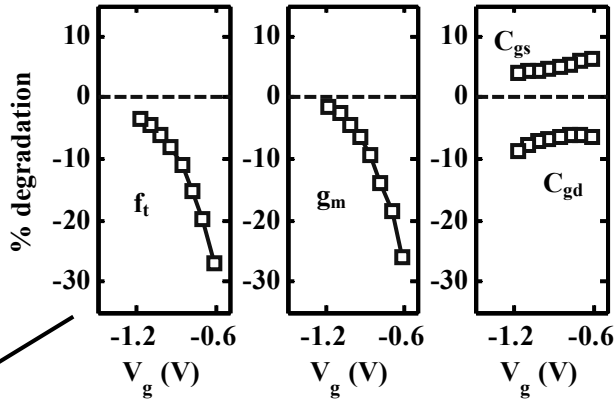

Fig. 6 The comparison of the degradation of f_t, g_m and C_{gs} after 1000s stress. The lower degradation of f_t at higher gate voltage can be explained by lower reduction of g_m and C_{gd} at this gate voltage.

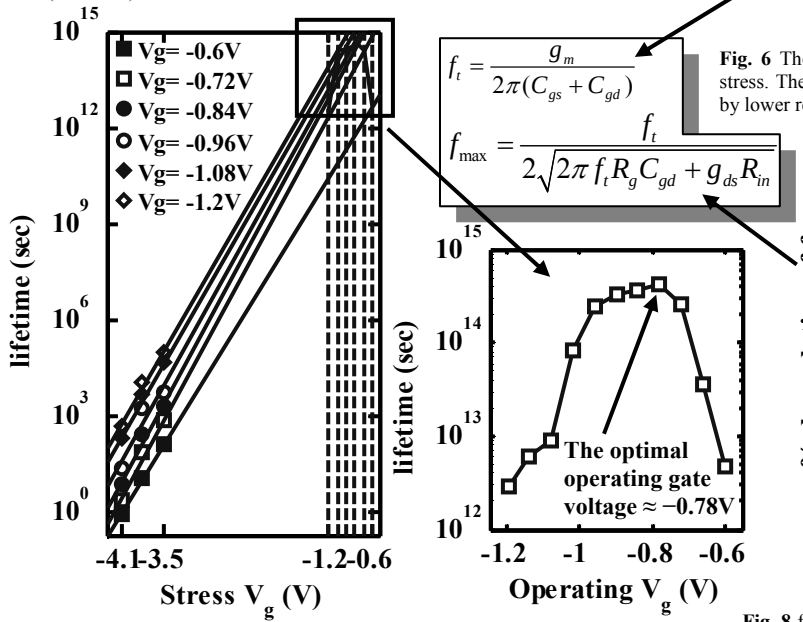

Fig. 7 The extrapolated lifetime versus gate voltage. Based on the measured results, the optimal operating gate voltage is extracted to maximize the lifetime of RF MOSFETs.

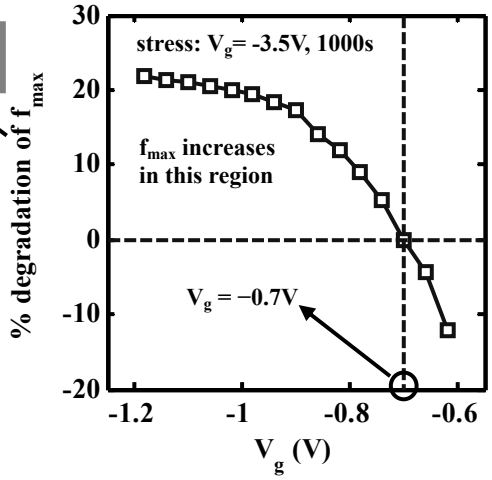

Fig. 8 f_{max} measured at different gate voltage. F_{max} measured at the gate voltage of -0.7V keeps unchanged after stress, which means the decrease of C_{gd} can exactly compensate the impact of the degradation of current gain and f_t on power gain and f_{max} at this bias point.