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Effects of Negative Bias Temperature Stress-induced Degradation and Mismatch on pMOSFETs in 90 nm Technology

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1. Introduction

It is well-known that the important reliability issues include drain avalanche hot-carrier (DAHC), channel hot-carrier (CHC), and negative bias temperature instability (NBTI). Early researches reported that pMOSFETs showed the worst degradation at DAHC and room temperature if cryogenic operation is unnecessary [1-2], but, based on 0.13 μm technology, our recent study showed that the worst case of HC has switched from DAHC to CHC and from low to high temperature. And the mechanisms pMOSFETs' degradation are related to bias temperature instability (BTI) effect plus reverse temperature effect [3-4]. Presently, NBTI-induced pMOSFET degradation is becoming more serious as feature dimension is continuously shrinking [5-7]. NBTI becomes the popular reliability issue in future CMOS applications.

Also, the matching of electrical properties between the identical transistor pairs on the same dice is important for wafer manufacturers and circuit designers. The foregoing reliability issues are the critical factor to induce transistor mismatches. An early study indicated that the mismatches of nMOSFETs' current gain factors (β, $\beta=\mu_n C_{ox}$W/L) and threshold voltage (V_t) due to HC stress in nMOSFETs of one dimension were reported increase monotonously with stress time [8], that implying HC-induced device mismatches have a large impact on the reliability of devices and circuits. Later, the mismatches of n- and pMOSFETs after DAHC were investigated [9]. Its results showed that the matching properties of nMOSFETs were rapidly becoming worse, but the changes were small for pMOSFETs. Further, there were other reports revealed that worse condition of HC effects on pMOSFETs have occurred in CHC at high temperature [4]. NBTI appears even worse than CHC at high temperature [10]. So, the severity of pMOSFET mismatches subjected to both CHC and NBTI stress should be understood.

In this work, NBTI-induced degradation and mismatch on 90 nm node pMOSFETs with SiON are thoroughly investigated. The degradation mechanism is speculated with gated-diode method. Further, mismatching properties of pMOSFETs with various sizes are compared after CHC and NBTI stress.

2. Experiments and result discussions

NBTI was applied on pMOSFETs having 16, 31 and 68 Å SiON oxide thickness (T_{ox}) and W/L = 10/10 (μm). Gated-diode (GD) method is utilized to analyze the degradation mechanism. For mismatching experiment, each of pMOSFET pairs is adjacent to each other with 16Å SiON and a minimum gate length of 90 nm. In total, 30 pairs with gate area (WL) =100, 3, and 0.9 (μm^2) on a same wafer were stressed to investigate CHC and NBTI effects. Tables 1 and 2 summarized the experimental conditions.

For NBTI-induced pMOSFET degradation, pMOSFETs with 68 Å SiON showed more severe V_{tlin} shifts as in Fig. 1, which contradicts with conventional thoughts. It is speculated that nitrogen incorporation into gate dielectric made NBTI worse although it increases dielectric constant and reduces boron penetration.

Figs. 2 and 3 illustrate recombination-generation (R-G) currents of GD measurements for pMOSFETs with 31 Å SiON at 25 and 125 ℃. Large amount of interface state (N_{it}) dominates at 125 ℃ while only the increment of oxide trapped charges (ΔN_{ot}) after NBTI at 25 ℃. Figs. 4 to 5 show R-G currents for pMOSFETs with 68 Å SiON at 25 and 125 ℃. Larger ΔN_{ot} is observed as SiON thickness of pMOSFETs increases from 31 to 68 Å. From Figs. 2 to 5, it is found that NBTI-induced N_{it} generation is strongly dependent of temperature. Although GD measurement results are not available for the device with 16 Å SiON due to unnegligible gate leakage current, it's presumed that pMOSFETs with 16 Å SiON exhibits similar degradation mechanism as pMOSFETs with 31Å SiON.

Then, using the lifetime model provided from [10], Fig. 6 shows the predicted lifetimes of pMOSFETs with different T_{ox} after NBTI. Note that the pMOSFETs with thinner gate oxide have lesser predicted lifetime although its degradation is smaller at the same electric field as shown in Fig. 1.

For stress-induced pMOSFET mismatch, according to the established model [11], transistor variability is expressed in terms of $1/\sqrt{WL}$. Fig. 7 shows standard deviation σ of ΔV_{tlin} for tested pairs of different gate areas after CHC and NBTI. The results reveal that small size device has the largest variation. Furthermore, the ratio R of σ(ΔV_{tlin}) of after- and before-stress shows that the mismatches after CHC are apparently worse than those of NBTI.

Fig. 8 illustrates the V_{tlin} shifts of different size devices are presented versus stress time during CHC and NBTI stress. In Fig. 8, CHC-induced degradation strongly aggravated as channel length (L) became shorter. For NBTI, the degradation seems to be independent of L. The degradation can be modeled in terms of exponential of time. n values of CHC and NBTI effects are about 0.27 and 0.26 respectively for the smallest size devices. This suggests that the mechanism of CHC-induced the degradation may be similar to that of NBTI for the small size devices. Based on a previous report [4], the probable mechanism is suggested to involve the creation of N_{it} owing to the integration of HC and NBTI effects.

Fig. 9 shows the comparisons of σ(ΔV_{tlin}) for device sizes of W/L = 10/10 and 10/0.09 (μm). The results exhibit that the mismatches enhanced as the device size is shrinking. For NBTI, it's likely unclear for the relation between transistor mismatches and stress time. Stress time should be extended to observe the mismatches after NBTI. Interestingly, CHC-induced the mismatches are worse than those of NBTI after time point of 3000 s, particularly for small size device. It may become a critical issue in future CMOS applications. Moreover, the cause of stress-induced mismatch is presumed that random traps generate in SiON dielectric and at SiON/Si-bulk interface [12].

3. Conclusions

In this work, it is to thoroughly investigate NBTI-induced pMOSFET degradation and mismatch in 90 nm technology. For NBTI-induced degradation, by using gated-diode measurement, the results show that the variation of N_{it} is apparently dependent on temperature. Further, the degradation is the worst on pMOSFETs with thicker SiON. It is because nitrogen incorporates into gate dielectric made NBTI worse. For stress-induced transistor mismatch, the results show that CHC mode is more serious than that of NBTI. It is suggested that CHC involves the integration of HC and NBTI effects to increase transistor mismatch, particularly for small size devices. Furthermore, the probable mechanism of transistor mismatch is due to the creation of random traps in SiON dielectric and at SiON/Si-bulk interface.

References

[1] M. Song et al., IEEE Electron Devices **44** (1997) 268.

[2] N. Koike et al., IEEE Device and Materials Reliability **4** (2004) 457.

[3] J. C. Lin et al., Japanese Journal of Applied Physics **45** (2006) 3144.

[4] S. Y. Chen et al., Japanese Journal of Applied Physics **47**,(2008) 1527.

[5] G. Chen et al., IEEE Electron Device Letters **23**, (2002) 734.

[6] Deter K. Schroder et al., Journal of Applied Physics **94** (2003) 1.

[7] H. Aono et al., Microelectronics Reliability **45** (2005) 1109.

[8] Y. Chen et al., IEEE Int. Integrated Reliability Workshop (2001) 41.

[9] S. Y. Chen et al., Japanese Journal of Applied Physics **45** (2006) 3266.

[10] C. H. Tu et al., Applied Surface Science **254** (2008) 6186.

[11] M. J. M. Pelgrom et al., IEEE Journal Solid-State Circuits **24** (1989) 1433.

[12] S. Pae et al., IEEE Trans. on Device and Materials Reliability **8** (2008) 519.

Table 1. NBTI stress conditions.

Width/Length (μm)	10/10		
T_{ox} (Å)	16	31	68
$E_{ox,stress}$ (MV/cm)	-10.3		
Temperature (°C)	25 , 75, 125		
Stress time (s)	to 10000		

Table 2. Mismatch experimental conditions.

Gate area, WL (μm^2)	100, 3, 0.9
V_{tlin} criterion	$V_g@I_{dlin}$=100 nA*W/L
T_{ox} (Å)	16
CHC $V_g=V_d=V_{stress}$ (V) NBTI $V_g=V_{stress}$ (V)	-2
Temperature (℃)	125
Stress time (s)	3000 for CHC 10000 for NBTI

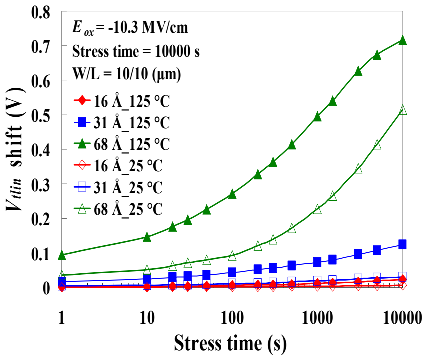

Fig. 1. V_{tlin} shifts of pMOSFETs with different T_{ox} after NBTI versus stress time at 25 and 125 ℃.

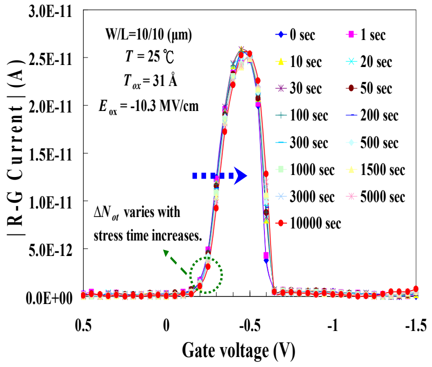

Fig. 2. R-G currents of pMOSFETs with 31 Å SiON after NBTI at 25 ℃.

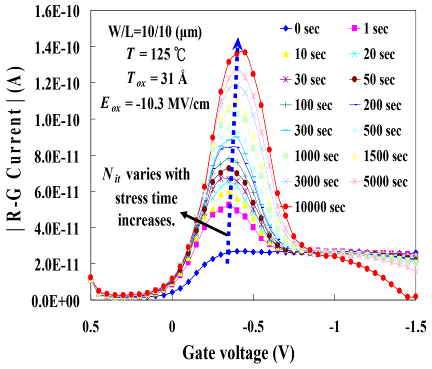

Fig. 3. R-G currents of pMOSFETs with 31 Å SiON after NBTI at 125 ℃.

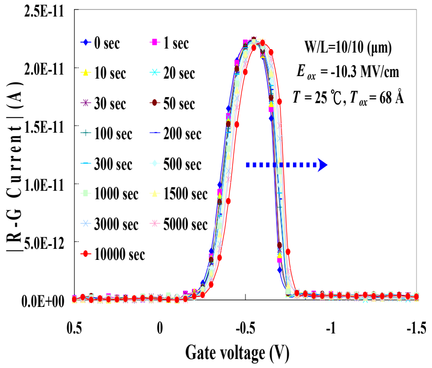

Fig. 4. R-G currents of pMOSFETs with 68 Å SiON after NBTI at 25 ℃.

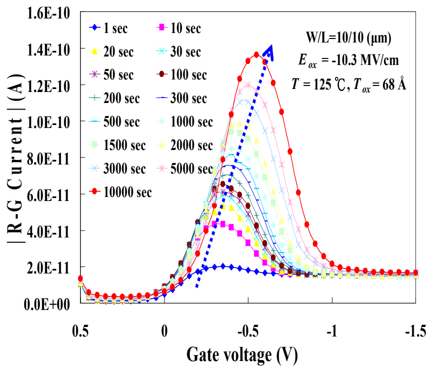

Fig. 5. R-G currents of pMOSFETs with 68 Å SiON after NBTI at 125 ℃.

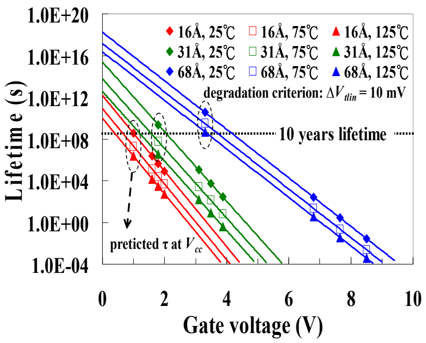

Fig. 6. The predicted lifetimes (10 years) of pMOSFETs with different T_{ox}.

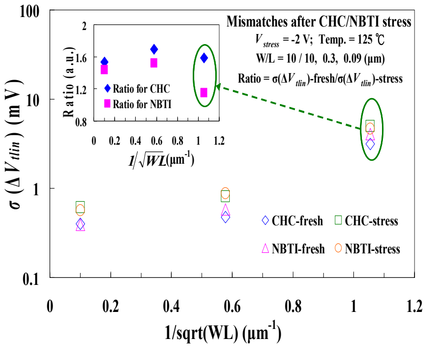

Fig. 7. σ(ΔV_{tlin}) of transistor pairs versus 1/sqrt(WL) ($1/\sqrt{WL}$ (gate area)) after CHC and NBTI. “fresh” and “stress” mean before- and after-stress respectively.

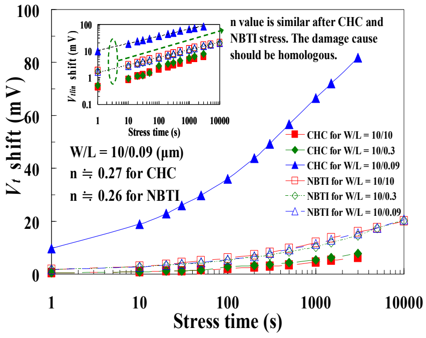

Fig. 8. V_{tlin} shifts for transistor pairs versus stress time after CHC and NBTI.

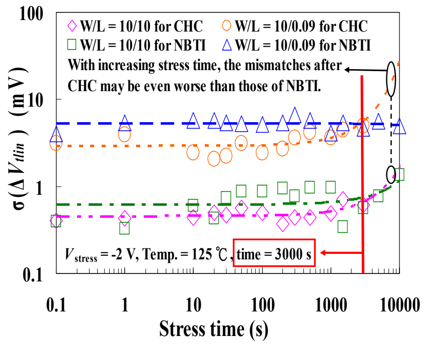

Fig. 9. Time history of the mismatches of σ(ΔV_{tlin}) for comparisons between the largest size device and the smallest size device.