Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp402-403

Subcircuit Compact Model for Dopant-Segregated Schottky Silicon-Nanowire MOSFETs

Guojun Zhu[1], Xing Zhou[1], Yoke King Chin[1], Kin Leong Pey[1], Guan Huei See[2], Shihuan Lin[1], Junbin Zhang[1], and Zuhui Chen[1]

[1]School of Electrical and Electronic Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798. E-mail: exzhou@ntu.edu.sg
[2]Chartered Semiconductor Manufacturing, Singapore 738406

1. Introduction

As conventional bulk-MOSFETs are approaching the end of the technology roadmap, MOSFETs with Schottky-barrier (SB) source/drain (S/D) are viewed as very promising candidates due to their low parasitic S/D resistance, superior scalability and low thermal budge [1]. However, due to the existence of the SB at S/D junctions, the drive current of SB MOSFETs is lower than its conventional counterparts while the leakage is much larger. To improve the performance the SB MOSFETs, dopant-segregation (DS) techniques [2] have been widely used. Due to the coupling of tunneling-thermionic (TT) and drift-diffusion (DD) carrier transport, formulation of analytical device models for dopant-segregated Schottky (DSS) MOSFETs is nontrivial and no analytical models are available so far.

In this paper, we demonstrate analytical device models and a novel subcircuit approach to physically and accurately model the DSS silicon-nanowire (SiNW) MOSFETs. The model is verified with both TCAD and experimental data. Very good agreement is achieved and the unique convex curvature in the I_D–V_D characteristics for DSS MOSFETs is accurately captured.

2. Modeling approach

The schematic of an ideal DSS SiNW MOSFET is shown in Fig. 1. The characteristics of DSS SiNW MOSFETs are found to be very sensitive to the physical parameters such as the length and dopant concentration in the segregation region. Carrier transport could be TT dominant or DD dominant, or a combination of both, which depends on the DS-related parameters. For either TT or DD dominant carrier transport, compact models have been developed by the authors to fully characterize the corresponding devices [3], [4]. For devices in which carrier transport is dominated by both TT and DD mechanisms, we propose a novel subcircuit approach, which is able to accurately model the unique convex curvature in the I_D–V_D characteristics.

The DSS device can be conceptually separated into two components: a Schottky diode at the S/D junction and an intrinsic silicon channel. The diode current consists of both thermionic and tunneling currents. The thermionic current is given as

$$I_{th} = AA^*T^2 \exp\left(-\frac{\Phi_{B,s(d)}}{v_{th}}\right)\left[\exp\left(\frac{V'_{s(d)} - RI_{th}}{nv_{th}}\right) - 1\right] \qquad (1)$$

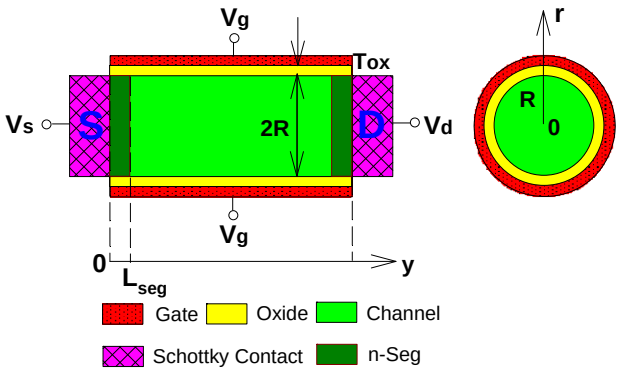

Fig. 1. Schematic of an ideal SB SiNW MOSFET: cross sections (left) along S/D and (right) along radial.

where A is the SB contact area and A^* is the effective Richardson constant. $\phi_{B,s(d)}$ is the Schottky barrier height (SBH) at the source (drain) junction and n is the ideality factor, which is treated as a fitting parameter. $V'_{s(d)}$ is the internal voltage between the SB and intrinsic channel.

The tunneling current is given as [5]

$$I_{tun} = A\frac{q^2F^2}{8\pi h\Phi_{B,s(d)}}\exp\left(-\frac{8\pi}{3hq|F|}\sqrt{2m^*\left(q\Phi_{B,s(d)}\right)^3}\right) \qquad (2)$$

where h is the Planck constant, m^* is the electron effective mass, F is the electric field at the metal-semiconductor interface.

The DD current in the intrinsic channel is given as

$$I_{ch} = 2\mu C_{ox}\frac{\pi R}{L}\left(V_{gf} - \overline{\phi_s} + 2v_{th}\right)V_{ds,eff} \qquad (3)$$

in which μ is the carrier mobility, $V_{gf} \equiv V_g - V_{FB}$ is the flat-band-shifted gate voltage and $C_{ox} = \varepsilon_{ox}/[R\ln(1 + T_{ox}/R)]$ is the cylindrical gate-oxide capacitance. $V_{ds,eff}$ is the effective terminal drain–source voltage including velocity saturation effect. ϕ_s is the surface potential. All major short-channel effects have been built into the core model.

The current continuity requires that

$$I_{ch} = I_{th} + I_{tun}. \qquad (4)$$

To solve the above equation, we adopt a subcircuit approach. Both the Schottky-diode model and channel-current model are separately implemented in Hspice using Verilog A, which can be simulated to obtain the internal node voltage $V'_{s(d)}$. The subcircuit is shown in the Fig. 2 inset.

3. Results and Discussion

Fig. 2 shows the model comparison with the measurement data for the devices with and without DS. For devices without DS, ambipolar transport is clearly observed and the

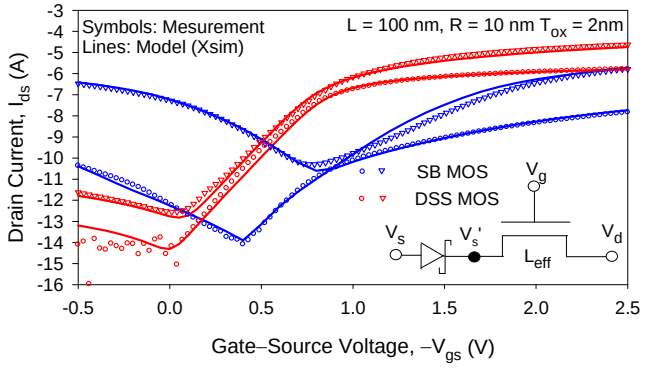

Fig. 2. Model (lines) comparison with measurement data (symbols) for both SB MOSFETs and DSS p-type MOSFETs at V_{ds} = –0.05 V and –1 V The subcircuit is shown in the inset

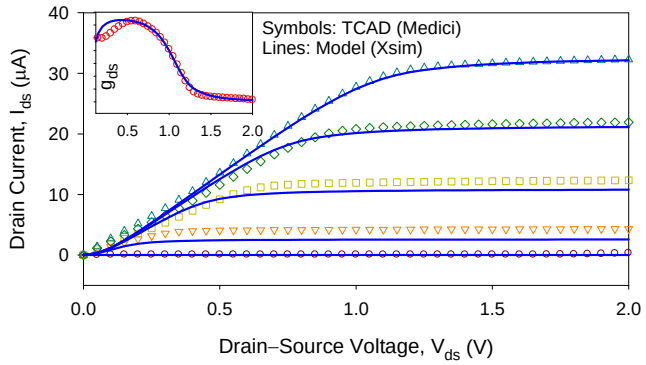

Fig. 3. Model (lines) comparison with TCAD (symbols) simulation for DSS MOSFETs. Output conductance is given in the inset which shows the negative curvature.

characteristics can be modeled by the SB-MOSFET model [3]. For the short-channel DSS p-type MOSFETs, the characteristics are modeled using the aforementioned subcircuit approach.

Fig. 3 shows the model comparison with TCAD (Medici) simulation, in which a midgap work function is used for the SB junction at S/D. The unique convex curvature in DSS I_D–V_D can be seen from the output conductance (Fig. 3 inset) and well reproduced by the model. Such characteristics are different from those of either SB or conventional MOSFETs.

Fig. 4 shows the model comparison with the measured data for two p-type DSS devices on the same wafer. The segregation length in the first device is long and the device shows the conventional DD characteristics as given in Fig. 4(a). For the second device, the characteristic falls in between the SB MOSFETs and conventional MOSFETs. By using the subcircuit approach, the unique convex curvature is well reproduced, which can be further justified from the characteristics of the output conductance of the two devices as shown in Fig. 4(c).

4. Conclusions

In conclusion, we have demonstrated the characteristics of the DSS MOSFETs, which are well reproduced by the proposed analytical model. The unique convex curvature in the I_D–V_D characteristics is accurately captured by using a

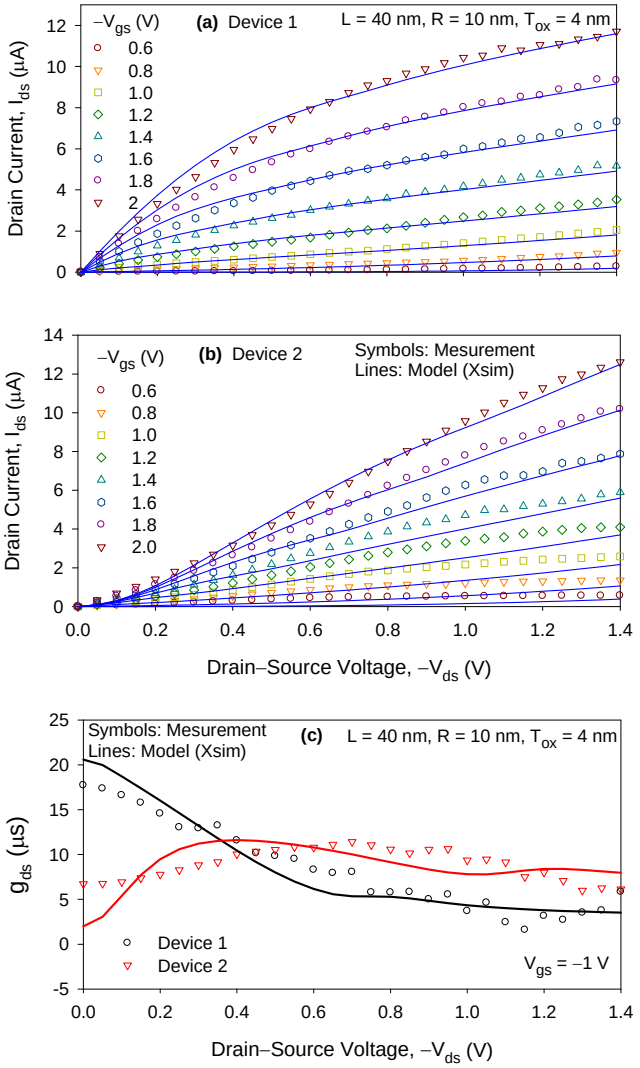

Fig. 4. Model (lines) comparison with measurement data (symbols) for two DSS devices: device 1 (a) and device 2 (b). Output conductances of the two devices are given in (c).

novel subcircuit approach. The modeling approach has been verified with both TCAD simulation and experimental data with excellent agreement.

Acknowledgements

This work was supported in part by Nanyang Technological University under Grant RGM30/03 and in part by Semiconductor Research Corporation under Grant 2004-VJ-1166G.

References

[1] J. M. Larson and J. P. Snyder, *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1048–1058, May 2006.

[2] R. A. Vega and T.-J. K. Liu, *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2665–2677, Oct. 2008.

[3] G. J. Zhu, X. Zhou, T. S. Lee, L. K. Ang, G. H. See, S. H. Lin, Y. K. Chin, and K. L. Pey, *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1100–1109, May 2009.

[4] G. J. Zhu, G. H. See, S. H. Lin, and X. Zhou, *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2526–2530, Sep. 2008.

[5] M. Jang, K. Kang, S. Lee, and K. Park, *Appl. Phys. Lett.*, vol.. 2, no. 16, pp. 2718–2720, Apr. 2003.