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Intrinsic-Parameter-Fluctuated Power-Delay Characteristics in 16-nm-Metal-Gate CMOS Devices and Circuits

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1. Introduction

CMOS device with metal gate is one of key technologies for the reduction of intrinsic parameter fluctuations. However, the use of metal as a gate material introduces a new source of random variation due to the dependency of workfunction on the orientation of metal grains [1-2]. In this work, we for the first time estimate the impact of the intrinsic parameter fluctuations consisting of metal gate workfunction fluctuation (WKF), process variation effect (PVE) and random dopant fluctuation (RDF) on 16-nm-gate CMOS devices and circuits. The fluctuations of the delay time, the static power, the dynamic power, and the short circuit power are investigated. Our preliminary results show that the delay time is impacted by the WKF and RDF due to the significant threshold voltage fluctuations (σV_{th}). The total power fluctuation of the planar MOSFETs is about 15.2%, which may induce significant performance degradation and uncertainty of CMOS circuits and systems. Additionally, though the static power is not an important part of the total power, it contributes a significant power fluctuation due to the serious leakage current fluctuation. This study assesses the intrinsic parameter fluctuations on nano-CMOS circuit's performance and reliability, which can in turn optimize designs of circuit and system.

2. Methodology and Results

The devices we investigated is the 16-nm-gate bulk MOSFETs (width: 16 nm) with amorphous-based TiN/HfSiON gate stacks and an EOT of 1.2 nm. The nominal channel doping concentrations are $1.48\text{x}10^{18}$ cm^{-3} and the V_{th} is calibrated. For RDF, 758 dopants are randomly generated in a large cube, in which the equivalent doping concentration is $1.48\text{x}10^{18}$ cm^{-3}, as shown in Fig. 1(a). The large cube is then partitioned into 125 sub-cubes. The number of dopants may vary from 0 to 14, and the average number is 6, as shown in Figs. 1(b), 1(c), and 1(d). These 125 sub-cubes are equivalently mapped into the device channel for the 3D quantum drift-diffusion device simulation with discrete dopants, as shown in Fig. 1(e) [3-5]. For WKF, considering the size of metal grains and the gate area of the devices, the device gate area is composed of a small number of grains. A statistically-sound Monte-Carlo approach is advanced here for examining such distribution, as shown in Fig. 1(f). The grain orientation of each parts and total gate workfunction are estimated based on properties of metal, as shown in Fig. 1(g) [1-2]. Figure 1(h) illustrates the estimation of gate length deviation and the line edge roughness induced fluctuations, whose magnitude follow the projections of the ITRS 2007. CMOS inverter is tested, as shown in Fig. 1(i). The circuit characteristics are obtained by coupled device-circuit simulation running on our parallel computation system [4-5].

Figures 2(a) and 2(b) present the V_{th} fluctuations for the NMOSFETs and PMOSFETs in this study. The total V_{th} fluctuation ($\sigma V_{th,total}$) is given by, according to the independency of the fluctuation components, $\sigma V_{th,total} = [(\sigma V_{th,PVE})^2 + (\sigma V_{th,WKF})^2 + (\sigma V_{th,RDF})^2]^{0.5}$). The $\sigma V_{th,RDF}$, $\sigma V_{th,WKF}$, and $\sigma V_{th,PVE}$, are the PVE-, WKF-, and RDF-induced V_{th} fluctuation, respectively. The RDF dominates the V_{th} fluctuation in NMOSFETs; however, for the V_{th} fluctuation of PMOS, the WKF becomes the dominating factor because of the large deviation of the workfunction for different grain orientation. Figures 3(a)-3(c) explores the WKF-, PVE-, and RDF-fluctuated gate capacitance (C_g) as a function of gate voltage (V_G). The solid line shows the nominal case and the dashed lines are the devices with intrinsic parameter fluctuations. The gate capacitance fluctuations (σC_g) with different V_G are summarized in Fig. 3(d). Different to the results of V_{th} fluctuation, the WKF brought less impact on gate capacitance fluctuation due to the screening effect of the inversion layer. The RDF and PVE dominate the gate capacitance fluctuations at 0.5V and 1.0V gate biases, respectively. The screening effect of the inversion layer reduces the impact of RDF at high gate bias; however, the screening effect is weakened by discrete dopants positioned near the channel surface. The PVE brings direct impact on the gate length and is independent of screening effect, which should be noticed when the transistor operated in high gate bias. Figures 4(a) and 4(b) presents the high-to-low delay time (t_{HL}) and low-to-high delay time (t_{LH}) characteristics of the studied inverters. Since the t_{HL} and t_{LH} are dependent on the V_{th} of NMOS and PMOS, respectively. The delay time fluctuations follow the σV_{th} as studied in Fig. 2. The delay time is significantly impacted by the WKF and RDF. Notably, the WKF shows an increasing importance in nanoscale transistor, especially in PMOSFETs due to different grain orientation in scaled gate area.

Figure 5 estimates the nominal power dissipation of inverter circuit. The total power (P_{total}) is consisted of the dynamic power (P_{dyn}), the short circuit power (P_{sc}), and the static power (P_{stat}). Their definitions are shown in the inset of Fig. 5. We herein use the transistors' gate capacitance as the load capacitance and focused on the device intrinsic parameter fluctuation induced circuit variability. The $f_{0->1}$ is the clock rate. I_{sc} is the short circuit current, which is observed as both NMOSFET and PMOSET turned on resulting a DC path between the power rails. T is the switching period. $I_{leakage}$ is the leakage current that flows between the power rails in the absence of switching activity. The P_{dyn} and P_{sc} are the dominating factors in power dissipation and P_{stat} seems insignificant in total power. The importance of P_{stat} is then explored in the Fig. 6. Figures 6(a)-6(d) summarize the intrinsic parameter fluctuation induced power fluctuations, σP_{dyn}, σP_{sc}, and σP_{stat}, respectively. The σP_{dyn} is resulted from the gate capacitance fluctuation and the σP_{sc} is induced by σV_{th}. Since there is an exponential relationship between the leakage current and the V_{th}, the significant leakage current fluctuation contributes an amazing static power fluctuation. Additionally, the σP_{total} ($\sigma P_{total} = [(\sigma P_{PVE})^2 + (\sigma P_{WKF})^2 + (\sigma P_{RDF})^2]^{0.5}$) is about 15.2% of the total power ($\sigma P_{total} / P_{total} = 0.0564 / 0.37$), which impacts the reliability of circuits and systems.

3. Conclusions

This work has reported the delay and power fluctuations of the 16-nm-metal-gate CMOS circuits. The intrinsic parameter fluctuations of the metal-gate devices have been extensively studied. The WKF plays an increasing important role in V_{th} fluctuation due to the scaled gate area and the large workfunction difference. The delay time is significantly impacted by the WKF and RDF and the trend of delay time fluctuation follows the σV_{th}. The CMOS circuits present a 15.2% power fluctuation, which may induce significant performance degradation and uncertainty of circuits and systems. Though the static power is not an important part of total power, it contributes a significant power fluctuation due to the significantly leakage current fluctuation.

Acknowledgement

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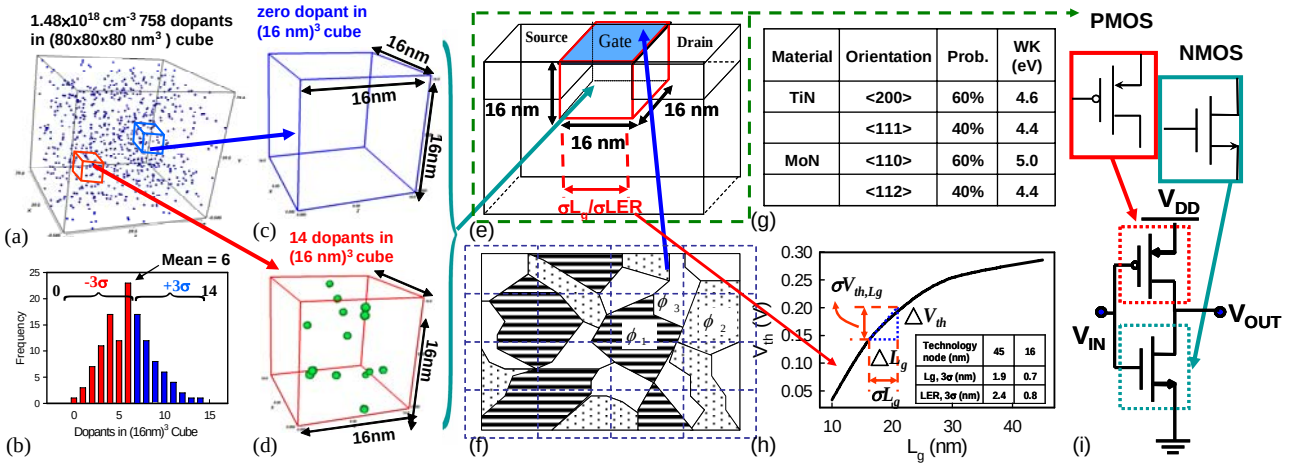

Figure 1. (a) 758 dopants are randomly generated in a large cube of 80x80x80 nm^3, in which the equivalent doping concentration is $1.48x10^{18}$ cm^{-3}. The large cube is then partitioned into 125 sub-cubes of 16x16x16 nm^3. The number of dopants in sub-cube may vary from 0 to 14, and the average number is 6 ((b)-(d)). These 125 sub-cubes are equivalently mapped into the device channel of bulk planar MOSFETs for the 3D device simulation with discrete dopants (see (e)). (g) The gate area of nanoscale devices is composed of a small number of grains and the distribution follows (f). (h) The estimation of PVE induced σV_{th}. (i) The tested inverter in this study.

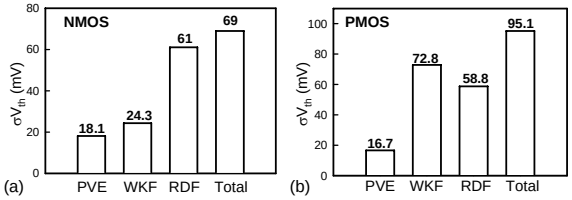

Figure 2. The summarized V_{th} fluctuation for (a) NMOSFETs and (b) PMOSFETs.

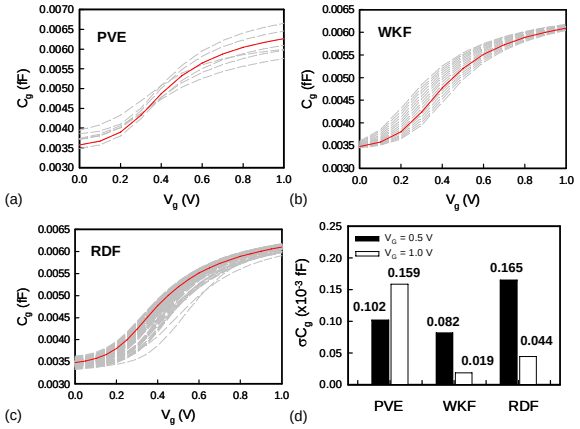

Fig. 3. The C_g-V_G characteristics with (a) PVE, (b) WKF, and (c) RDF. (d) The C_g fluctuation for 16-nm-gate MOSFETs with WKF, PVE, and RDF. The filled-in bars are the results of V_G = 0.5 V and the open bars are the results of V_G = 1 V.

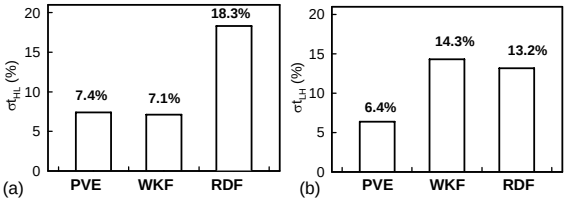

Fig. 4. The normalized fluctuations (standard deviation/nominal value) of (b) t_{HL} and (c) t_{LH} with respect to WKF, PVE, and RDF for the planar CMOS.

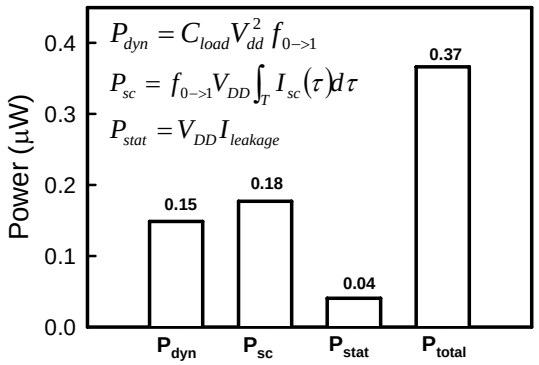

Fig. 5. The nominal power for the bulk planar MOSFET circuits.

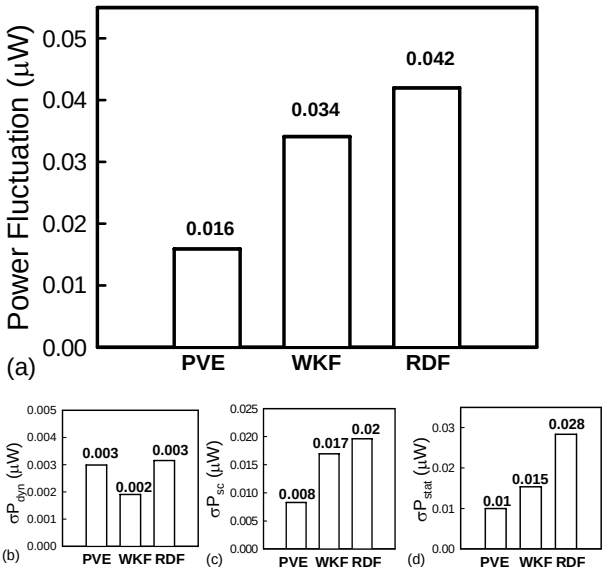

Fig. 6. The summarized (a) power, (b) dynamic power, (c) short circuit power, and (d) static power dissipation fluctuations.