Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp406-407

Carrier Transportation of ALD HfLaO Gate Dielectrics with 0.72 nm EOT

H. W. Chen[1], Y. W. Liao [1], S. Y. Chen[1], C. H. Liu[2, *], H. S. Huang[1],
L. W. Cheng[3, **], C. T. Lin[3], and G. H. Ma[3],

[1]Institute of Mechatronic Engineering, National Taipei University of Technology, Taiwan
[2] Dept. of Mechatronic Technology, National Taiwan Normal University
[3]Central R&D Division, United Microelectronics Corp. (UMC), Taiwan
[*]Tel.: +886-2-23583221 ext. 12, Fax: +886-2-23583074, E-mail: liuch@ntnu.edu.tw
[**]Tel.: +886-3-5782258, Fax: +886-3-5797246, E-mail: lwcheng@umc.com.tw

1. Introduction

Recently, many high-κ thin films have been extensively studied for the application of 45 nm generation and beyond.[1-4] Among various potential high-κ thin films, HfO_2-based materials are very promising due to relatively high dielectric constant (16~30),[1-2] acceptable bandgap (5.1~6.0 eV),[1-2] and acceptable dielectric breakdown field.[1-2] However, pure HfO_2 thin films have encountered a serious problem, low crystallization temperature (~500 ℃)[3], which would induce nonuniform interfacial layer, threshold voltage instability, and defect generation.[4-5] In the literature, Si, N, Al, or Ta has been incorporated into HfO_2 gate dielectrics to increase the crystallization temperature.[4-7] Although these additives can improve crystallization temperature with good thermal stability, their dielectric constants and the barrier heights at gate/dielectric or dielectric/substrate are reduced in comparison with pure HfO_2.[4-7] Therefore, the gate leakage current increases compared to pure HfO_2 thin films with the same equivalent oxide thickness (EOT). Recently, lanthanum (La) has been incorporated into HfO_2 thin film due to the following reasons: (1) the tunability of the V_{FB} and V_T by unpinning the Fermi level, (2) no degradation of the dielectric permittivity of HfO_2 thin films, (3) the increased crystallization temperature, and (4) the improved PBTI effects.[8-9] However, carrier transportation in LaO/HfO_2 stacked gate dielectrics have not been studied in detail.

2. Experiments and Results

All test devices were fabricated at UMC using 90 nm technology-node process. *P*-type silicon (*p*-Si) wafers were used as the starting substrate. After the standard RCA cleaning procedures, 2 nm ALD HfO_2 thin film was performed, followed by 1 nm ALD LaO thin film. Then, a 10-nm TaC metal gate was deposited by PVD as the gate electrode. Finally, a post-metal-anneal (PMA) was employed at 420℃ in forming gas for 30 min. The fabrication flows of the samples are shown in Fig. 1. The EOT and V_{FB} are extracted from CVC model of NCSU with quantum effects taken into consideration.

The inset of Fig. 2 is the structure of TaC/LaO/HfO_2/*p*-Si capacitors. Fig. 2 shows the high-frequency (100k Hz) and simulated *C*-*V* characteristics. The dielectric constant and EOT are determined to be about 16.3 and 0.72 nm, respectively. The D_{it} is extracted to be about 1.4×10^{11} ev^{-1}-cm^{-2} near midgap using Terman method.[10] The dielectric breakdown field is around 12.3 MV/cm at room temperature, as shown in Fig. 3. In order to analyze the carrier transportation of the LaO/HfO_2-stacked thin films, the temperature dependence of the gate leakage current (J_g) has been extensively carried out in this work. Fig. 4 shows the J_g-E characteristics from 300 to 500 K. The J_g is about 6.8×10^{-2} A/cm^2 at V_{FB} - 1 V. Fig. 5 further compares the J_g (@ $V_g = V_{FB}$ - 1 V) versus EOT characteristics among SiO_2, HfO_2, HfSiON, HfLaO, $HfZrO_4$, and LaO/HfO_2 (this work), and some important parameters are summarized in Table Ⅰ.[1,11-13] It's clear that the 0.72 nm EOT LaO/HfO_2 stacked dielectric is superior in J_g-EOT characteristics to the other dielectrics. The outstanding J_g versus EOT characteristics of ALD LaO/HfO_2 stacked gate dielectric suggests its excellent scalability for future gate-dielectric applications.

After analysis, the main carrier transportation is found to be Schottky emission or Poole-Frankel (P-F) emission. It is well known that the most likely carrier transportation in gate dielectrics is Schottky emission which can be expressed as,[14-15]

$$J_{SE} = A^* T^2 \exp[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0})}{k_B T}], \quad [1]$$

For a typical Schottky emission, a plot of $\ln(J/T^2)$ versus $E^{1/2}$ would yield a straight line. The experimental data in the region of the high temperatures (450~500 K) and low to medium electric fields (0.20~0.93 MV/cm) fit the Schottky emission theory very well under gate injection as shown in Fig. 6 (a). The fitted dynamic dielectric constants (ε_r) are determined to be between 5.06 and 5.66. Therefore, the Schottky barrier height (Φ_B) at TaC and LaO interface is about 1.21±0.04 eV by making use of the so-called Arrhenius plot, as shown in Fig. 6 (b).

However, in the region of low temperatures (300~375 K) and medium to high electrical fields (1.93~2.73 MV/cm) under gate injection, the carrier transportation is dominated by P-F emission, which is a bulk-limited conduction. The leakage current in thin dielectric films associated with P-F emission can be determined by utilizing the following equation:[14-15]

$$J_{P-F} = C_1 E \exp[\frac{-q(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_0})}{k_B T}] \quad [2]$$

By the same token, for P-F emission, a plot of $\ln(J/E)$ versus $E^{1/2}$ should be linear. As shown in Fig. 7 (a), the experimental data in the region of the low temperatures (300~375 K) and medium to high electric fields (1.93~2.73 MV/cm) under gate injection are best described by the P-F emission. The ε_r are between 5.11 and 5.52. Moreover, the trap energy level (Φ_t) in the LaO/HfO_2 stacked structure is extracted to be about 0.51±0.03 eV, again from the Arrhenius plot as shown in Fig. 7 (b). It should be noted that the barrier heights discussed in this work are effective values, meaning that the effects of interfacial layer (IL) are included.

3. Conclusions

In this article, MOS capacitors incorporating ALD LaO/HfO_2 stacked gate dielectrics with metal gate (TaC) were fabricated and investigated. The experimental results reveal that the EOT is 0.72 nm and the J_g is only 6.8×10^{-2} A/cm^2 at V_{FB} - 1 V. The excellent J_g versus EOT characteristics indicates that ALD LaO/HfO_2 stacked gate dielectric has outstanding scalability for future gate-dielectric applications. In the region of low to medium electric fields and high temperatures, the current conduction mechanism is governed by Schottky emission, while the dominant conduction mechanism is P-F emission in the region of medium to high electric fields and low temperatures. Moreover, the barrier height (Φ_B) is estimated to be about 1.21 eV at TaC and HfLaO interface, and the trap energy level (Φ_t) is found to be about 0.51 eV.

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- ***P*-Si (100)**
- **Standard RCA clean**
- **2 nm ALD HfO_2 gate dielectric**
- **1 nm ALD LaO gate dielectric**
- **10 nm PVD TaC gate electrode**
- **PMA (420 °C, 30 min in FG)**

Fig. 1. Fabrication flows of ALD LaO/HfO_2 stacked gate dielectric with metal gate (TaC).

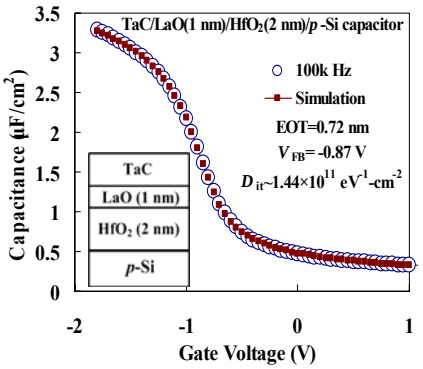


Fig. 2. *C-V* characteristics of TaC/LaO/HfO_2/*p*-Si capacitor. The inset shows the structure of the device in this work.

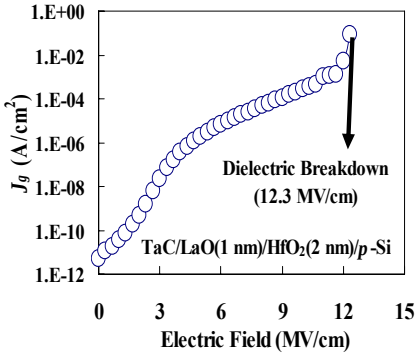


Fig. 3. *J-E* plot for breakdown characteristic of TaC/LaO/HfO_2/*p*-Si capacitor at room temperature.

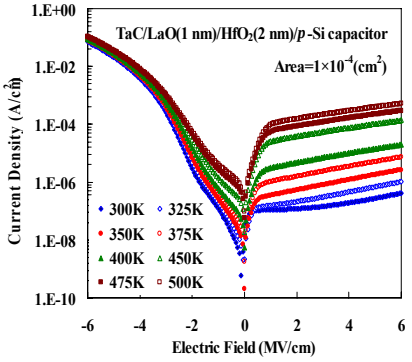


Fig. 4. *J-E* characteristics of TaC/LaO/HfO_2/*p*-Si capacitor from 300 to 500 K.

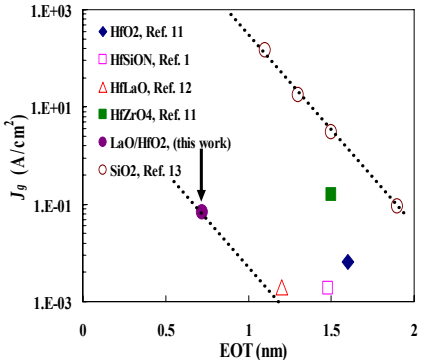
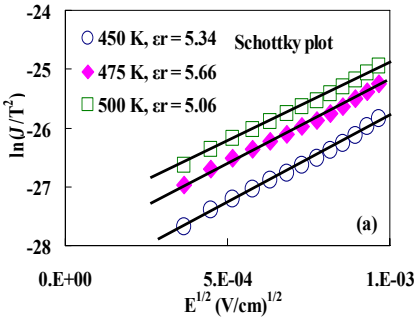


Fig. 5. Characteristics of J_g-EOT for SiO_2 and Hf-based high-κ dielectrics.

Table Ⅰ. A comparison of some important parameters with Hf-based thin films.

Gate oxide	EOT (nm)	J_g (A/cm^2)	D_{it} (cm^{-2}-eV^{-1})
HfSiON [1]	1.48	6.8×10^{-3}	2.7×10^{11}
$HfZrO_4$ [11]	1.5	0.16	N/A
HfO_2 [12]	1.6	6.5×10^{-3}	N/A
HfLaO [12]	1.2	2×10^{-3}	N/A
LaO/HfO_2 (This work)	0.72	6.8×10^{-2}	1.4×10^{11}



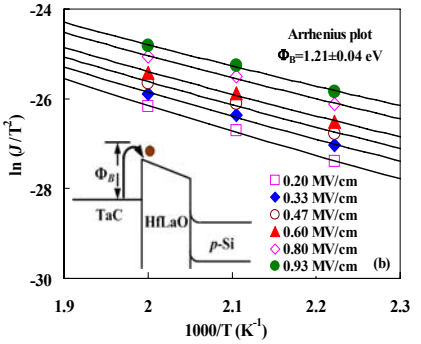
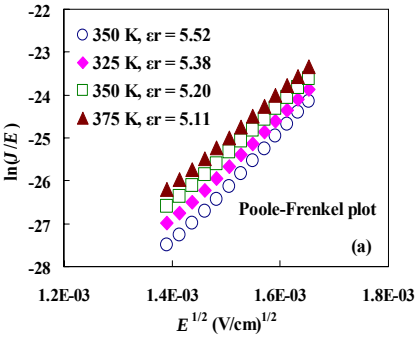


Fig. 6. (a) Schottky emission plots in the region of high temperatures and low to medium electric fields. (b) Arrhenius plots for Schottky emission at various electric fields. The inset of Fig. 6 (b) is the band diagram of the TaC/HfLaO/*p*-Si structure.



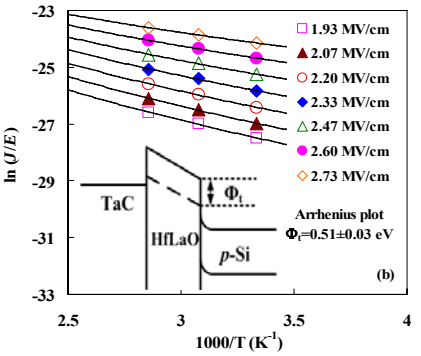


Fig. 7. (a) P-F emission plots in the region of low temperatures and medium to high electric fields. (b) Arrhenius plots for P-F emission at various electric fields. The inset of Fig. 7 (b) is the band diagram of the TaC/HfLaO/*p*-Si structure.