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The Structure and Power-level Dependences of CMOS RF Power Cell Degradation by Hot-carrier Stress with Load Pull System

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1. Introduction

With the development of CMOS process, the scale of the channel length of MOSFET is reduced from um to nm. But some critical reliability issues come with the scaled-down. The hot-carrier effect is induced by the lateral electrical field between the drain to source of a MOSFET [1]. The carriers in the channel with enough energy which is larger than the bandgap of gate oxide will induce some traps or interface states near the drain. The hot-carrier effect makes the shift of threshold voltage, degradation of drain and tranconductance (gm) [2]. These degradations of dc characteristics will also affect the RF performances of the devices. By measuring the degradation of the drain current, the reliability of devices could be considered.

In a high frequency device, the reflected power is induced from load mismatch and may transfer to heat or be absorbed by the carriers near the drain side of MOSFET. With the energy increasing, more carriers will trap into the gate dielectric or induce more interface states. This phenomenon makes the hot-carrier effect heavier. So the hot-carrier effect is one of the most important reliability issues in advanced CMOS technology, especially in high power applications.

In this work, the structure and power-level dependences of hot-carrier effect in power cells are discussed.

2. Experiments

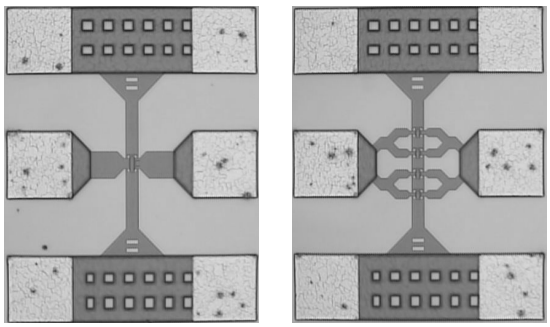
The power cells were fabricated with TSMC 0.18μm triple-well 1P6M CMOS technology. The studied cells were designed with unit fingers in parallel. The channel length and width of each unit finger is 0.18 and 5um, respectively. The designed bias condition is V_{GS} of 1.2 V and V_{DS} of 1.8 V. Two sets of cells were designed for output power of 10 mW and 50 mW at 5.2GHz.

DC and RF stresses

In this work, two experiments were done. For DC stress, the cell was biased at high voltage with V_{GS} of 1.8 V and V_{DS} of 2.5 V. Under DC stress, the current density and lateral electrical field increase to expedite the hot-carrier effect. For RF stress, the input power was set to be 0 dBm with designed bias condition. At output terminal, the reflection power was induced with load mismatch by setting load reflection coefficient, Γ_L. In RF stress, the influence of reflected power in hot-carrier effect could be discussed. The Load-Pull system with MAURY 982B01 tuners is used to set the load impedance and desired reflection coefficient. The on-wafer DC characteristics were measured by using an Agilent 4142B Modular DC Source/Monitor.

Set 1: Power cells for output power of 10mW

Figure 1 shows the photographs of the studied power cells for output power of 10mW. Cell 1 is a 16-finger transistor module. Cell 2 consists of four dispersive 4-finger transistor modules connected in parallel. The total channel widths of these two cells are both 80 um. The measured dc current of both fresh cells is about 24.5 mA.



(a) (b)

Fig. 1 Photograph of (a) Cell 1: 16 fingers (b) Cell 2: four transistors with 4 fingers in parallel.

In RF stress, the load mismatch was done with the reflection coefficient of 0.351∟-40.33°. The degeneration degrees of DC drain current of cell 1 and 2 were shown in Figure 2. The degradations of DC stress in these two cells were similar. But after RF stress, cell 1 suffered from larger degradation. The degradation degree from load mismatch was 8.6% for cell 1 and 5.5% for cell 2 after 70 minutes.

Set 2: Power cells for output power of 50mW

Figure 3 is the photographs of the studied power cells for output power of 50mW. Cell 3 is one 64-finger transistor module. Cell 4 consists of four dispersive 16-finger

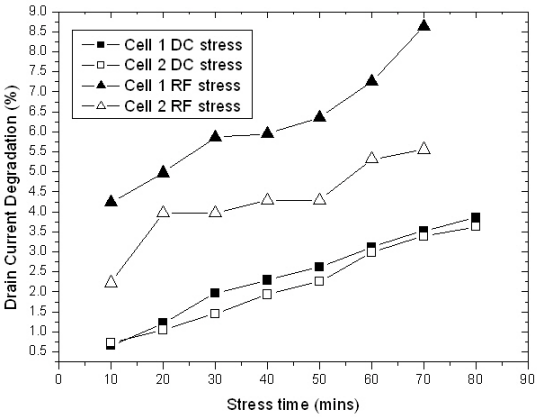
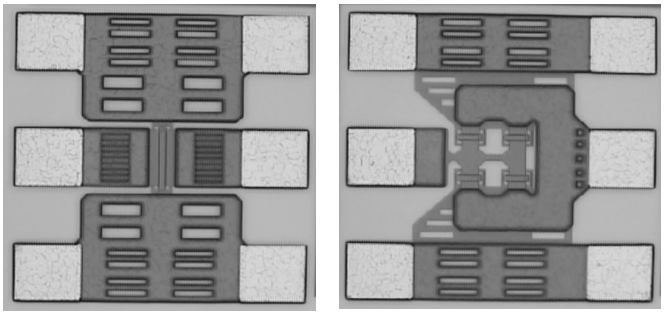


Fig. 2. Comparison of degradations of DC drain current after RF and DC stresses in cell 1 and 2.(Measured at V_{GS}=1.2V and V_{DS}=1.8V)

transistor modules connected in parallel. The total channel widths of these two cells are both 320 um. The measured dc current of both fresh cells is about 90 mA. With the consideration of high current density in these two cells, the line width to ground was larger than 100um.



(a) (b)

Fig. 3 Photograph of (a) Cell 3: 64 fingers (b) Cell 4: four transistors with 16 fingers in parallel.

For RF stress, the load reflection coefficient was set to be 0.7915∟-137.43°. Fig. 4. shows the comparison of DC and RF stresses in these two cells. It is also found that the degradation of cell 3 and 4 are similar under DC stress. The degradation of cell 3 under RF stress reached to 29.2% after 90 minutes compared to 19.8% of Cell 4. The output power of cell 3 decreased from 15.25 to 14.5 dBm after RF stress.

3. Discussions

From the measured results, some phenomena can be observed. First one is that the degradations of DC stress in both cells with the same total width were similar. This is because the current density and electrical field are the same under DC stress. The second one is that the hot-carrier effects under RF reflected power by load impedance mismatch is much larger than that of DC stress. The reason is that the reflected power increases the energy of hot carriers and makes the gate dielectric damaged more heavily. Compared the degradation in different layout

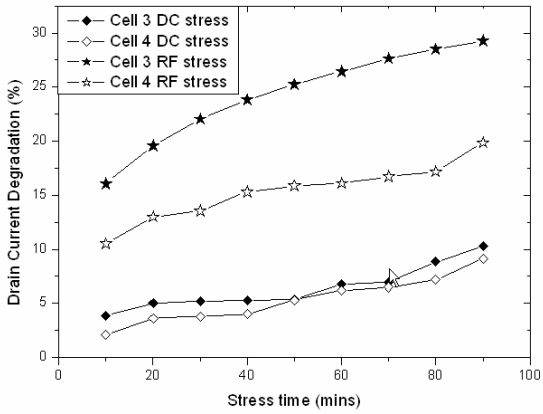


Fig. 4. Comparison of degradations of DC drain current after RF and DC stresses in cell 3 and 4.(Measured at V_{GS}=1.2V and V_{DS}=1.8V)

patterns, it is found that the degradation of RF stress is softened with dispersive layout structure. These three phenomena could be found in the two set of studied cells.

From the comparison of these two set of experiment, it is found that the power-level of studied cells dominates the degradation both in DC and RF stress. The designed output power for cell 3 and 4 is 50mW which is much larger than 10mW for cell 1 and 2. The heat will increase the temperature of cells and influences the hot-carrier effect because the fixed positive charge and the interface trap will be serious at high temperature [3]. Under load mismatch, cell 3 and 4 suffered from more reflected power which induced more degradation from hot-carrier effect.

3. Conclusion

In this work, two set of power cells under DC and RF stresses are measured. The results show the dependence of drain current degradation on structure and power-level of the designed power cells. The hot-carrier effect is the most important issue for advanced technology, especially in high power application. This work also suggests that the dispersive layout pattern could avoid heavy degradation from hot-carrier effect.

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