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Anomalous Hot-Carrier-Induced Saturation Drain Current Degradation in DEMOS Transistors

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1. Introduction

High-voltage drain-extended MOS (DEMOS) devices have been intensively used for the applications in flat panel display drivers and smart-power management [1]-[2]. One major reliability concern in DEMOS transistors is hot-carrier reliability because the devices are often operated under high drain voltage (V_d) and high gate voltage (V_g). Since hot-carrier-induced damage in most of the DEMOS devices is located in the drift region, on-resistance (R_{on}) degradation of the device is usually much greater than saturation drain current (I_{dsat}) degradation [3].

In this paper, the mechanism responsible for hot-carrier-induced device degradation in a 32V n-type DEMOS device is discussed. In addition, an unexpected high I_{dsat} degradation (close to R_{on} degradation) is observed in this 32V DEMOS device. According to data and simulation results, the mechanism responsible for such an anomalous I_{dsat} degradation is suggested.

2. Experiments

Fig. 1 shows the schematic cross section of the DEMOS transistor used in this work. The channel region (L_{ch}), accumulation region (L_{acc}), and gate overlapped shallow trench isolation (STI) region (L_s) are depicted. This device is fabricated with a 0.18μm CMOS process. The operational voltage of the device is 32V for both V_d and V_g. DC stressing with various V_g and V_d = 35.2V at room temperature is performed with the source and bulk connected to the ground. To extract stress-induced interface state formation (ΔN_{it}), charge pumping current (I_{cp}) is measured. The stress tests are interrupted periodically to measure the degradation of device parameters (including R_{on}, I_{dsat}, maximum transconductance G_{mmax}, threshold voltage V_T) and I_{cp}. R_{on} (= V_d/I_d) is measured at V_d = 0.1V and V_g = 32V. I_{dsat} is monitored when $V_d = V_g$ = 32V. G_{mmax} and V_T are extracted at V_d = 0.1V. TCAD simulation results including impact ionization rate and current flow are analyzed to examine the mechanism responsible for device degradation as well as the unexpected high I_{dsat} degradation.

3. Results and Discussion

To evaluate the effect of V_g on device degradation, devices are stressed under various V_g (ranging from 2V to 32V) at V_d = 35.2V. Stress results reveal that the V_g that produces the most R_{on} degradation is V_g = 32V. Thus, the following analysis is focused on the device stressed under V_g = 32V. Fig. 2 shows the degradation of device parameter during stress. R_{on} degrades much more seriously than G_{mmax}. Besides, V_T shift is small (< 10mV), revealing that stress-induced damage is mainly located in the N^- drift region. Note that the value of I_{dsat} degradation is close to R_{on} degradation. Such a trend is different from most of the hot-carrier-induced degradation in DEMOS devices where R_{on} degradation is much greater than I_{dsat} degradation [3].

To investigate the mechanism responsible for device degradation, the impact ionization rate along Si/SiO_2 interface is simulated. Results in Fig. 3 reveal that the maximum of impact ionization is located at the STI corner closest to the channel (i.e. Si/SiO_2 interface in L_s region). To experimentally locate the damage, ΔN_{it} in L_{ch}, L_{acc}, and L_s regions are extracted from I_{cp} data by the method proposed in [4]. Results in Fig. 4 show that ΔN_{it} in L_{ch} region is much smaller than ΔN_{it} in L_{acc} and L_s regions. This is consistent with the data in Fig. 2 that G_{mmax} degradation and V_T shift are small. For ΔN_{it} in L_{acc} and L_s regions, ΔN_{it} in L_s region is much greater than ΔN_{it} in L_{acc} region. Such a result suggests that the device degradation is mainly caused by ΔN_{it} in L_s region. This is also consistent with the simulation result in Fig. 3 that the impact ionization maximum is located in L_s region. To further verify whether device degradation is caused by ΔN_{it} in L_s region, the correlation between device degradation and ΔN_{it} in L_s region is investigated. As seen in Fig. 5, ΔN_{it} in L_s region correlates with R_{on} and I_{dsat} degradation well. According to results in Figs. 3–5, ΔN_{it} in L_s region is the main mechanism responsible for R_{on} and I_{dsat} degradation.

To examine the mechanism responsible for unexpected high I_{dsat} degradation, I_d vs. V_d characteristics of the device is shown in Fig. 6. When the measured V_g is lower (8, 16V), the saturation of I_d under high V_d bias is due to the pinch-off in the channel region. When the measured V_g is higher (24, 32V), the increase of saturation I_d becomes less evident because the saturation of I_d under high V_d bias is caused by carrier velocity saturation in the drift region rather than by conventional pinch-off in the channel region. Such a phenomenon is known as quasi-saturation [5]-[6]. To investigate the effect of quasi-saturation on device degradation, I_d degradation ($\Delta I_d/I_d$) measured at V_d = 32V with measured V_g as a parameter is analyzed. As seen in Fig. 7, $\Delta I_d/I_d$ is small when the measured V_g is lower. However, $\Delta I_d/I_d$ is significant when the measured V_g is higher. To understand the effect of measured V_g on $\Delta I_d/I_d$, current flow of the device biased at low V_g (V_g = 8V) and high V_g (V_g = 32V) under V_d = 32V are simulated and shown in Fig. 8. When the measured V_g is low, the current flow in L_s region is distributed away from Si/SiO_2 interface due to channel pinch-off. Thus, ΔN_{it} in L_s region has small influence on $\Delta I_d/I_d$, resulting in small $\Delta I_d/I_d$. On the other hand, when the measured V_g is high (the device is operated under quasi-saturation region), the current flow in L_s region is close to Si/SiO_2 interface. Thus, ΔN_{it} in L_s region has severe impact on $\Delta I_d/I_d$ at high measured V_g. According to results in Figs. 6–8, the occurrence of quasi-saturation is the main mechanism responsible for unexpected high I_{dsat} degradation.

4. Conclusions

The mechanism of hot-carrier-induced degradation in our DEMOS transistor is identified to be ΔN_{it} in L_s region. Our findings also reveal that unexpected high I_{dsat} degradation is observed in devices that exhibit quasi-saturation phenomenon. Such anomalous I_{dsat} degradation should be paid special attention in evaluating hot-carrier reliability of DEMOS transistors.

References

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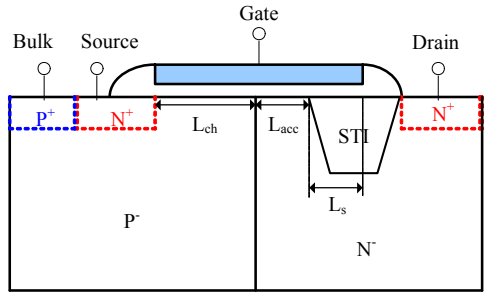

Fig. 1 The structure of DEMOS transistors used in this work.

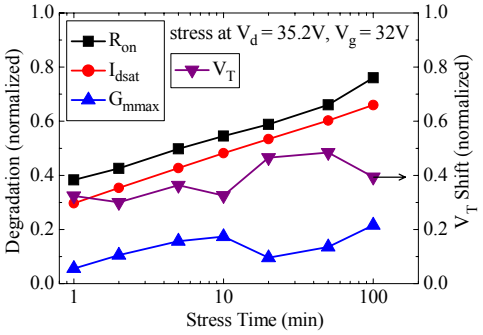

Fig. 2 Device degradation data show that the value of I_{dsat} degradation is close to R_{on} degradation.

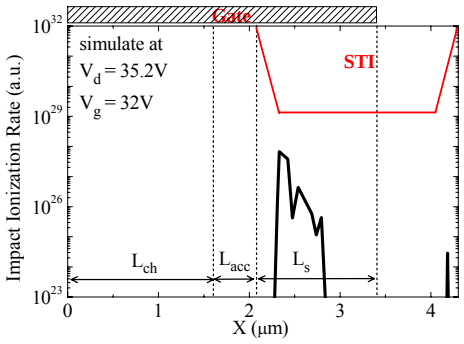

Fig. 3 Simulation results show that the maximum of impact ionization rate along Si/SiO_2 interface is located at L_s region.

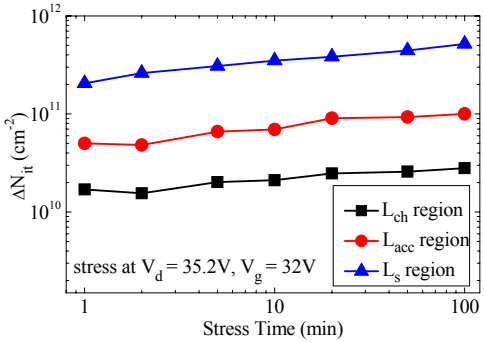

Fig. 4 The extracted ΔN_{it} data reveal that ΔN_{it} in L_s region is much greater than ΔN_{it} in L_{ch} and L_{acc} regions.

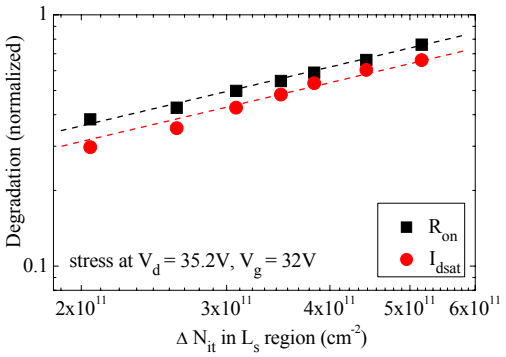

Fig. 5 ΔN_{it} in L_s region correlates with R_{on} and I_{dsat} degradation well.

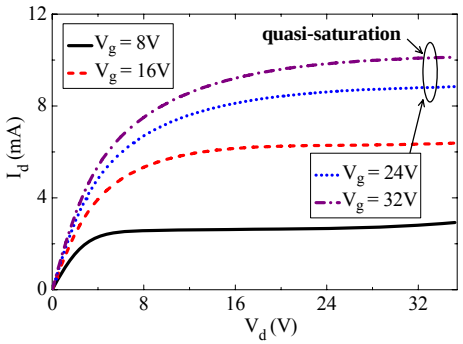

Fig. 6 Increase of saturation I_d is less evident when the measured V_g is higher, revealing the occurrence of quasi-saturation.

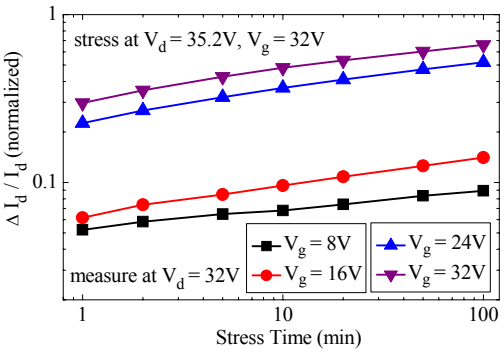

Fig. 7 $\Delta I_d/I_d$ is small when the measured V_g is lower, however, $\Delta I_d/I_d$ is significant when the measured V_g is higher.

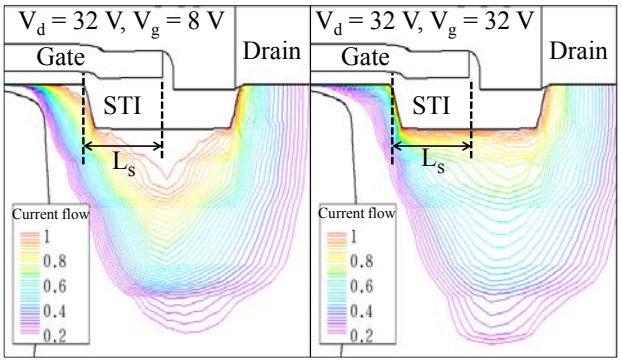

Fig. 8 Current flow of the device biased at V_g = 8V and 32V when V_d = 32V. The current flow is close to Si/SiO_2 interface in L_s region when the device is biased at V_g = 32V.