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Subthreshold SRAM with Enhanced Stability using Ultra-Thin-Body and BOX SOI

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1. Introduction

The large fraction of chip area often devoted to SRAM makes low power SRAM design very important for ultra-low power applications, such as portable devices, implanted medical instruments, and wireless sensor networks. Subthreshold operation is an efficient technique to achieve ultra-low power consumption for circuits by lowering the power supply (Vdd) below the threshold voltage [1]. Conventional 6T bulk subthreshold SRAM cells face many challenges with increasing process variations in deep sub-100nm technologies [2-4]. Various 8T [2] and 10T [3-4] bulk SRAM cells have been proposed to improve the stability in subthreshold region. Ultra-Thin-Body (UTB) SOI MOSFET with thin buried oxide (BOX) is very attractive for subthreshold circuit applications due to its better control of short-channel effects (SCEs), lower subthreshold swing, and reduced leakage and Random Dopant Fluctuation (RDF) resulting from the use of un-doped (or lightly-doped) thin silicon film. In this work, we analyze the stability of 6T UTB SOI subthreshold SRAM cells considering Line Edge Roughness (LER) which is the main source of variation in UTB SOI MOSFETs [5]. The advantages of using UTB SOI MOSFETs for subthreshold SRAM applications are also assessed.

2. Device Design and Characteristics

Fig.1 compares the I_d-V_g characteristics for 40nm bulk and UTB SOI MOSFETs under the same Idsat at V_d = 1.0V. The bulk MOSFET is designed with channel concentration (N_{ch}) = 3E18cm^{-3} to control the SCEs. As can be seen, with equal I_{on} at 1.0V, the I_{off} of the UTB SOI devices are about 2 orders of magnitude lower than their bulk counterparts. Fig. 2 and Fig. 3 show the I_d-V_g characteristics for UTB SOI MOSFETs considering LER and for bulk devices considering RDF, respectively. To assess the LER in UTB SOI MOSFETs, the line edge patterns were derived using the Fourier synthesis approach [6]. Monte Carlo simulations were then performed. To assess the RDF in bulk devices, atomistic device simulations using the Monte Carlo approach [7] were carried out. The subthreshold current spreading of bulk devices due to RDF at V_g = 0.2V is around 50X, significantly larger than that of about 20 for UTB SOI MOSFETs considering LER. Therefore, UTB SOI MOSFET shows better variation immunity than the bulk one. Fig. 4 compares the number of cells per bit-line for bulk and UTB SOI 6T SRAM cells versus I_{on}/I_{off} ratio based on the criterion that the total bit-line leakage be less than 10% of I_{on}. Due to better electrostatic integrity and lower subthreshold swing, UTB SOI MOSFETs with larger I_{on}/I_{off} ratio result in higher number of cells per bit-line than the bulk counterparts. Even considering the worst case I_{on}/I_{off} ratio due to LER, the UTB SOI SRAM can still support adequate number of cells per bit-line. On the contrary, the bulk SRAM with the worst case I_{on}/I_{off} ratio due to RDF may fail to deliver the density requirement.

3. Read Static Noise Margin

Static Noise Margin is a measure of SRAM cell's ability to maintain its data state. Mixed-mode device/circuit simulations [8] are used to examine the cell stability. Fig. 5 compares the nominal Read Static Noise Margin (RSNM) of 40nm UTB SOI and bulk 6T/8T SRAM cells as a function of Vdd. The UTB SOI 6T/8T SRAM cells show larger RSNM than the bulk counterparts. Fig. 6 shows the RSNM characteristics for 6T UTB SOI SRAM cells considering LER at Vdd = 0.4V. Fig. 7 shows the RSNM characteristics for 6T bulk SRAM cells considering RDF at Vdd = 0.4V. As can be seen, bulk devices with threshold voltage variations due to RDF result in significant mismatch of neighboring transistors in SRAM cells, thus severely degrading the cell stability, and there is no margin at all. On the other hand, UTB SOI MOSFETs with better variation immunity can still maintain adequate margin for subthreshold SRAM operation.

4. Write Static Noise Margin

Fig. 8 shows the Write Static Noise Margin (WSNM) comparison for bulk and UTB SOI 6T SRAM cells at Vdd = 0.4V. The UTB SOI SRAM cell shows comparable WSNM as compared with the bulk counterpart. Fig. 9 illustrates three circuit techniques to improve WSNM, including boosted word-line voltage (VWL), negative bit-line voltage (VBL) and lower cell supply voltage (VCS). Both boosted VWL and negative VBL increase the strength of the pass-gate access transistors (AL, AR) and improve WSNM. Lower VCS makes pull-up transistors (PL, PR) weaker to facilitate Write operation. Lower VCS also suppresses the latching effect that hinders Write operation. Figs. 10-12 demonstrate that using these three techniques, UTB SOI SRAM cells with lower subthreshold swing show larger improvement in WSNM as compared with the bulk SRAM cells. For WSNM improvement, both negative VBL and boosted VWL are more effective than lower VCS, and negative VBL shows larger improvement in WSNM than booted VWL.

5. Conclusions

The stability of SRAM cells operating in subthreshold region can be enhanced by using UTB SOI MOSFETs with thin BOX. UTB SOI MOSFETs with larger I_{on}/I_{off} ratio can maintain larger number of cells per bit-line even considering the worst case I_{on}/I_{off} ratio due to LER. UTB SOI 6T/8T SRAM cells show higher RSNM than bulk SRAM cells in subthreshold region. Even considering LER, the UTB SOI 6T SRAM cells still provide sufficient margin while the bulk 6T SRAM cells with RDF fail to maintain adequate margin. Techniques for improving WSNM such as negative VBL, boosted VWL and lower VCS are more effective for UTB SOI SRAM cells than bulk SRAM cells.

Acknowledgements

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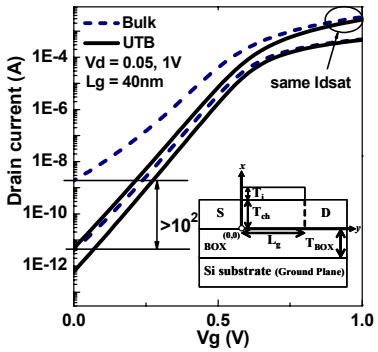

Fig.1. Comparison of I_d-V_g characteristics for 40nm bulk and UTB SOI MOSFETs. UTB SOI MOSFET is designed with N_{ch} = 1E16cm^{-3}, T_{ch} = 10nm, T_{BOX} = 10nm and EOT = 1nm. Insert shows the schematic sketch of UTB SOI MOSFET. Bulk device follows the prediction of 2007 ITRS with EOT = 1nm.

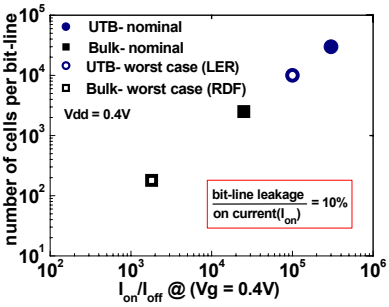

Fig.4. Comparison of number of cells per bit-line for bulk and UTB SOI SRAM.

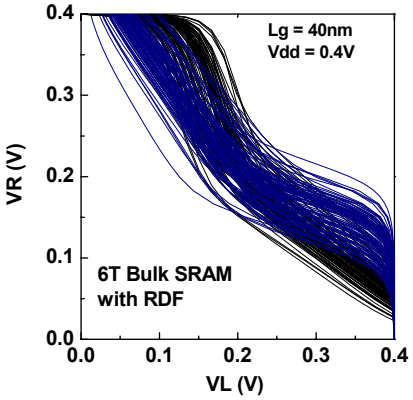

Fig. 7. RSNM characteristics for 6T bulk subthreshold SRAM with random dopant fluctuation.

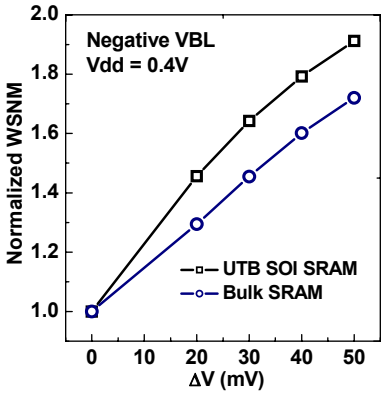

Fig. 10. Normalized WSNM comparisons between bulk and UTB SOI 6T subthreshold SRAM with negative VBL.

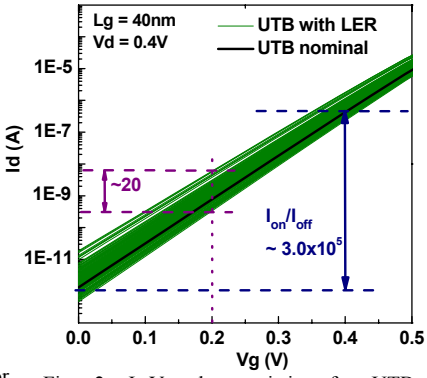

Fig. 2. I_d-V_g characteristics for UTB SOI MOSFETs with Line Edge Roughness. (correlation length: 30nm, rms amplitude: 1.5nm).

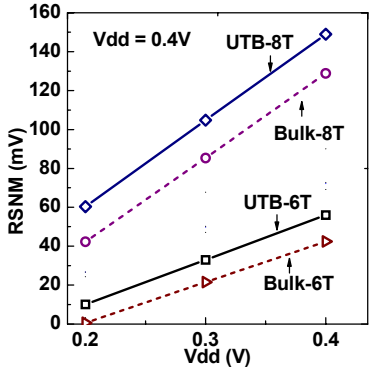

Fig. 5. 6T/8T RSNM comparisons of 40nm bulk and UTB SOI SRAM in subthreshold region.

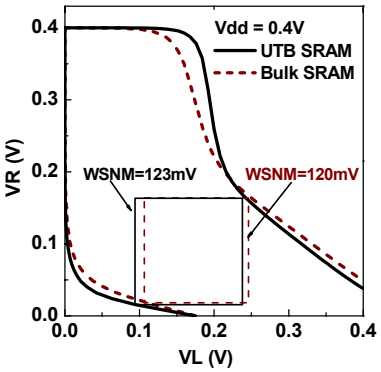

Fig. 8 WSNM characteristics comparison for bulk and UTB SOI SRAM cells at Vdd = 0.4V.

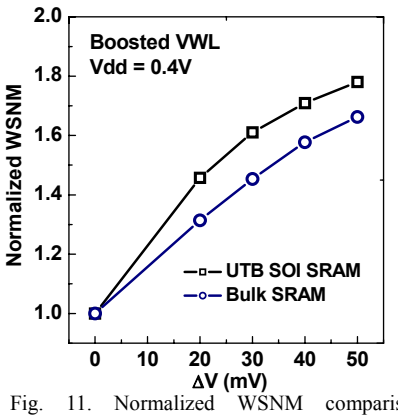

Fig. 11. Normalized WSNM comparisons between bulk and UTB SOI 6T subthreshold SRAM with boosted VWL.

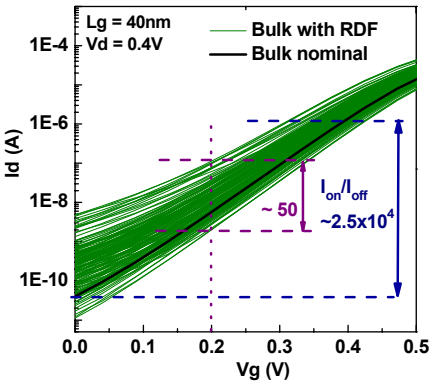

Fig. 3. I_d-V_g characteristics for bulk MOSFETs with Random Dopant Fluctuation.

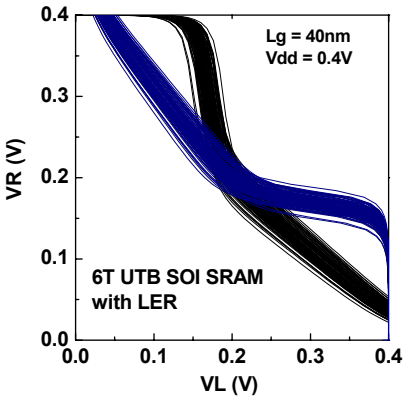

Fig. 6. RSNM characteristics for 6T UTB SOI subthreshold SRAM with line edge roughness. (correlation length: 30nm, rms amplitude: 1.5nm).

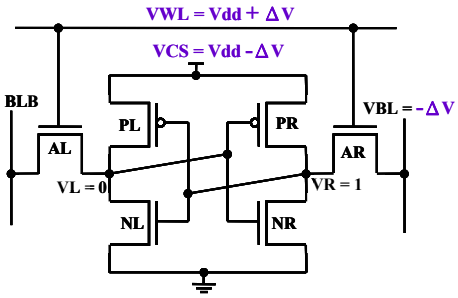

Fig. 9. Three circuit techniques to improve WSNM. (boosted VWL, negative VBL, and lower VCS).

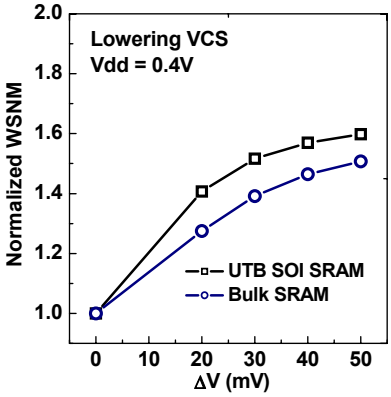

Fig. 12. Normalized WSNM comparisons between bulk and UTB SOI 6T subthreshold SRAM with lower VCS.