Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp380-381

Rigorous Design of 20 nm Level SOI 4-T FinFETs for Low Standby Power by Extracting Parameters from the Pre-stage 50 nm Technology Node Devices

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1. Introduction

Recently, managing the standby power is considered as a critical issue in high-density, mobile CMOS technology. One of the major leakage current sources in ultra small MOSFETs is gate-induced drain leakage (GIDL) caused by band-to-band tunneling (BBT) near the drain end [1]. Silicon-on-insulator (SOI) devices have advantages such as reduced intra-junction and punch-through leakage currents [2], and 4-termial (4-T) FinFETs have advantages of threshold voltage controllability and higher current drive. In this work, 20 nm level SOI 4-T FinFET is carried out suppressing GIDL varying underlap lengths by process/device simulations [3]. The embedded parameters were extracted from the device on pre-stage 50 nm technology node and the junction-engineered pn test element groups (TEGs).

2. Device Fabrication and Parameter Extractions

The schematic view and cross-section SEM image of the 50 nm device are shown in Fig. 1 [4]. For extracting the carrier lifetimes, pn TEGs were fabricated by the same processes for S/D formation of the device in Fig. 1. P-type SOI wafer with 5×10^{15}/cm^3 body doping was prepared. The 1000 Å thick active is mesa-isolated. 1000 Å TEOS was deposited and LDD was formed by ion implantation (IIP) with 5×10^{13}/cm^2 As^+, 5 keV, and 60° tilt. Sidewall was built by consecutive deposition and dry etch of Si_3N_4. Deep S/D IIP was performed with 1×10^{15}/cm^2 P^+, 10 keV, and 7° tilt. After RTA activation at 830 ℃ for 4 s, ILD was deposited and contact holes were dry-etched, which were followed by metallization and alloy. The junction-engineered pn TEG is shown in Fig. 2 (junction width=0.6~41.2 μm). The effective junction length (Fig. 3) was calculated from junction capacitance (Fig. 4) measured by Agilent 4284 A, which is 1.887×10^{-3} cm (Fig. 5). The carrier and generation lifetimes are calculated by following two equations [5]:

$$J_R = I_R / WL_{eff} = q\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A} + \frac{qn_iW_{dep}}{\tau_g}, \tau_g = \tau_p e^{(E_T-E_i)/kT} + \tau_n e^{-(E_T-E_i)/kT} \quad (1)$$

From the effective junction area and reverse currents at -0.2 V/-0.35 V measured by Agilent 4156C (Fig. 6) assuming E_T~E_i, the carrier lifetimes are extracted as $\tau_n=3.949\times10^{-9}$ s and $\tau_p=5.752\times10^{-6}$ s. The distances from n^+ peaks of LDD/deep S/D to metallurgical junction are 17/50 nm, respectively (Fig. 7). For more elaborate BBT model, the parameters are extracted from at standby condition: V_D=1.0 V, $V_{G,Drv}=V_{G,Ctr}$<0 V ($V_{G,Drv}$/$V_{G,Ctr}$: drive and control gate voltages). The tunneling generation rate is [6]:

$$G_{BBT} = \alpha E^{\gamma} \exp\left(-\frac{\beta}{E}\right) \quad (2)$$

The extracted parameters from measurement are $\alpha=8\times10^{14}$ cm^{-1}V^{-2}s^{-1}, $\beta=8.3\times10^6$ V/cm, and γ=2.0. Also, contact resistance and electron mobility parameters are extracted for on-current fitting. The modeling result is shown in Fig. 8.

3. Low Standby Power 20 nm SOI 4-T FinFET Design

Fig. 9 shows the I_D-$V_{G,Drv}$ curves for 20 nm device with reduced SOI thickness of 10 nm for gate controllability and 1 nm gate oxide thickness, where the drive/control gates are connected in common. Fig. 10 depicts threshold voltages with underlap length variation, which copes with the DG MOSFET requirements by technology roadmap [7]. On/off currents and ratio are shown in Fig. 11 and 12, respectively. The current ratio has a local maximum at underlap length of 15 nm. Fig. 13 demonstrates GIDL with underlap variation. GIDL is defined as the current difference as BBT model is turned on and off at V_{off} where I_D of 3 pA/μm is obtained without BBT model. If permissible GIDL is assumed as 1 pA/μm, the underlap length should be at least 10 nm. Therefore, for stable threshold voltage window under process variations and effective GIDL suppression, the underlap length should be around 15 nm. Fig. 14 shows the 4-T operation results with $V_{G,Ctr}$ biasing.

4. Conclusion

In this work, a low standby power 20 nm SOI 4-T FinFET has been designed with extracted parameters. For stable device performance and low standby power, the underlap length should be precisely controlled around 15 nm.

Acknowledgements

We thank Korea Science and Engineering Foundation (KOSEF) and Japan International Science and Technology Exchange Center (JISTEC) for the exchange research.

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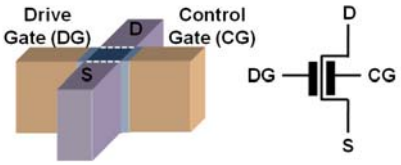
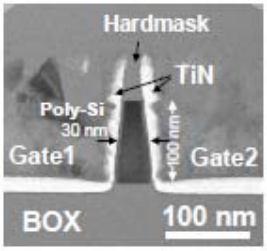


(a)



(b)

Fig. 1. 4-T SOI FinFET. (a) Schematic view and circuit unit (b) SEM image [4].

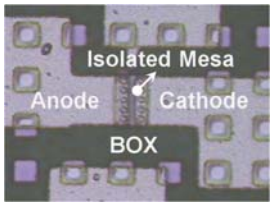


Fig. 2. Junction-engineered pn TEG.

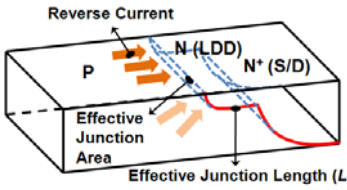


Fig. 3. Effective junction area of pn TEG.

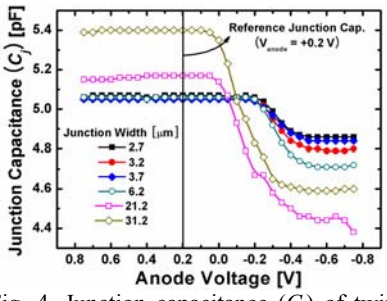


Fig. 4. Junction capacitance (C_j) of twin pn TEGs in parallel connection under the anode voltage sweep (forward to reverse).

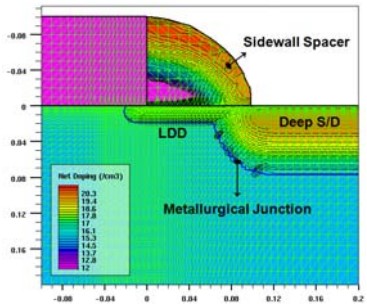


Fig. 5. Device structure and doping profiles made by ATHENA (units in μm).

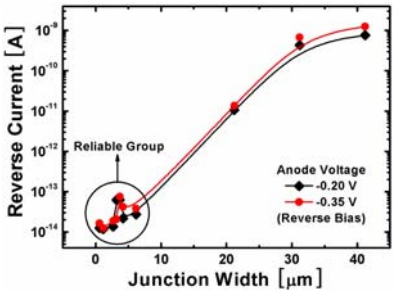


Fig. 6. Reverse current with junction width variation.

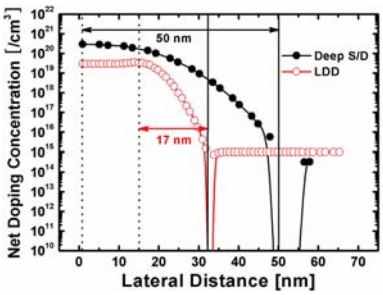


Fig. 7. Doping profiles and gradients near the junctions at LDD and deep S/D ends.

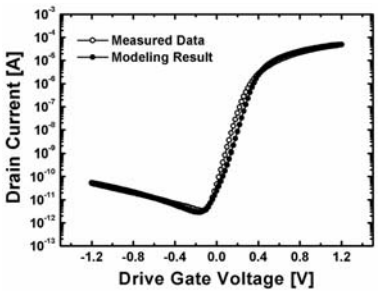


Fig. 8. Measured data and optimization of band-to-band tunneling model (V_D=1.0 V).

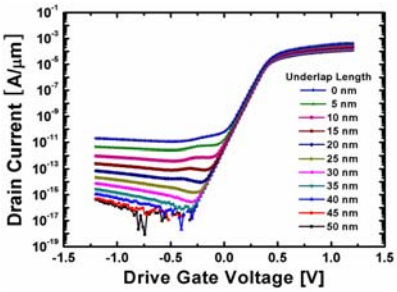


Fig. 9. I_D-$V_{G,Drv}$ curves for 20 nm device with underlap length variation (V_D=1.0 V).

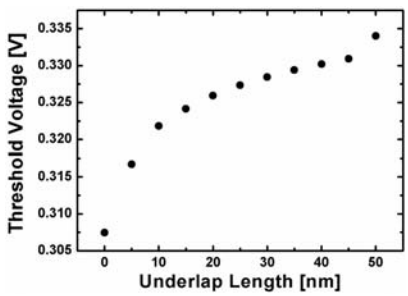


Fig. 10. Threshold voltages ($V_{G,Drv}$@I_D=1 μA/μm) with underlap length variation.

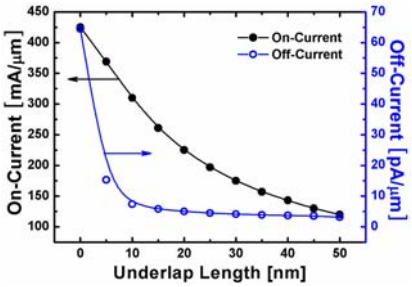


Fig. 11. I_{on} and I_{off} with underlap length variation (I_{off}=I_D@($V_{G,Drv}$,V_D)=(0 V,1 V)).

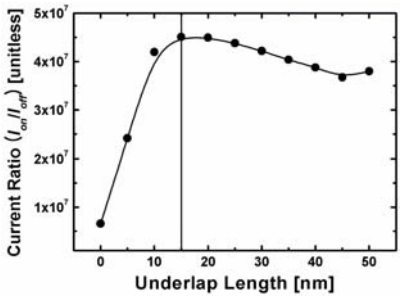


Fig. 12. Current ratio (I_{on}/I_{off}) with underlap length variation (maximum at 15 nm).

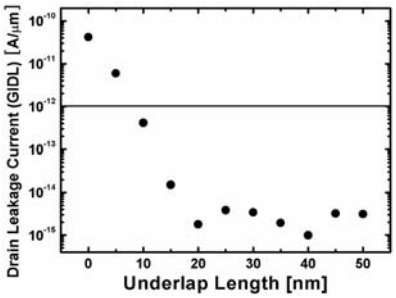
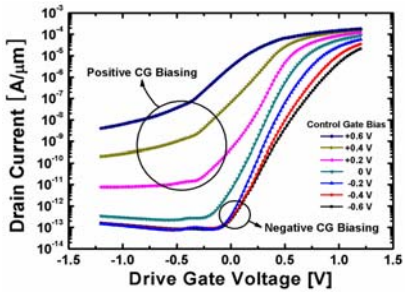
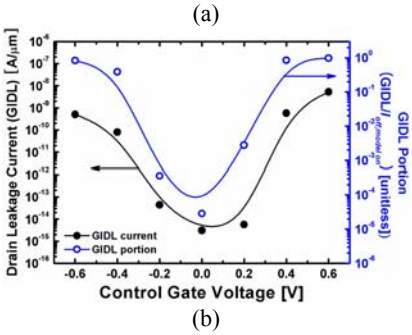


Fig. 13. GIDL with underlap length variation. Reference line indicates 1 pA/μm.



(a)



(b)

Fig. 14. Effects of control gate biasing. (a) I_D-$V_{G,Drv}$ curves (b) GIDL and portions (underlap length = 15 nm, V_D = 1.0 V).