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Low Frequency Noise *(1/f)* Improvements on CMOS Transistors with a Single n^+ Doped Poly Si-SiGe Gate Stack

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1. Introduction

When poly-Si is substituted by poly-SiGe as a gate material for the MOS transistors, it is well known that the polycrystalline silicon -germanium films (poly-SiGe) have the main advantages of good compatibility with standard CMOS process. Others advantages have also been reported [1] that (a) the dopant activation in poly-SiGe is comparable to poly-Si, (b) the workfuntion is decreasing with increase in the Ge mole fraction, (c) the workfunction change originates in band gap reduction caused mainly by the increase of the effective SiGe lattice constant. Furthermore, the literature [2] indicates that poly-SiGe can substitute poly-Si as a CMOS gate material for Ge mole fractions not exceeding 0.6 (for both n- and p-type gates) and that the technology is still in a developmental stage [3].

In this work, a comparative study of CMOS transistors fabricated in a conventional way (with poly-Si gate) and with two layers (poly-Si/SiGe) as a gate material is presented and we demonstrate that improvements in the CMOS transistors performance can be achieved by an engineering of gate workfunction.

The SiGe integration with local CMOS process was developed which uses a single n^+ doped, poly-$Si_{0.7}Ge_{0.3}$ gate material to achieve both n^+ doped gate n-MOS and n^+ doped gate p-MOS devices. The achieved reduction of gate depletion and improved DC characteristics agree with literature [4] [5] observing that this literature uses a single p^+ doped, poly-$Si_{1-x}Ge_x$ gate material. Furthermore, as gate oxide becomes thinner, the benefit of SiGe gate becomes more obvious.

For low noise evaluation purpose, the devices were biased in low regime and examined the low-frequency noise (1/f) based on the method reported in literature [6].

2. Device Fabrication

A total of 57 steps of process were required for our standard CMOS, including a total of 8 photolithography steps, as described in references [7]. An integration scheme required after gate oxide some additional steps of process. A 30nm gate TCE oxide was grown at 1000°C and then followed by the deposition of 500nm undoped poly-Si and of 100nm undoped SiGe as gate layers. The undoped poly-SiGe films used throughout this work were deposited by low-pressure chemical vapor deposition (LPCVD) using SiH_4 and GeH_4 as the sources. Details of our local technique to overcome the problem of growing undoped SiGe and Poly-Si layer structures were reported elsewhere [8].

3. Device Characteristics

The CMOS transistors were fabricated to demonstrate the advantages of using poly $Si_{1-x}Ge_x$ as the gate material, using CCS standard 2μm CMOS process. Since it is advisable for RF design, a low gate voltage biasing with same drain current level, it required that the poly-Si/SiGe gate p or n-MOSFETs have output conductance and peak transconductance G_m improved when compared to poly-Si gate MOSFETs. The observed increase in G_m value indicates an improvement due to poly-Si/SiGe gate and this behavior is noticeable in the n-MOS device characteristics shown in figure 1.

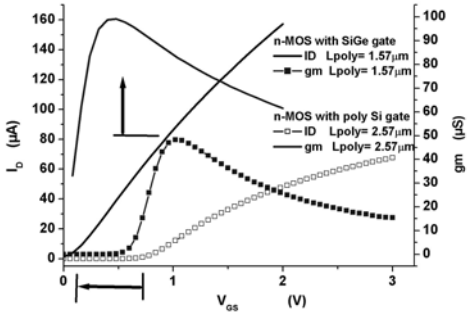

Fig. 1 Threshold characteristics for two n-MOSFETs devices with the same size of W=20μm, L=1.57μm at V_{DS} = 0.1V with SiGe gate (solid lines) and with poly-Si gate (dot lines) L_{poly}=2.57μm.

The p-MOSFETs of W=20μm, L_{poly}=1.57μm at V_{DS}= -0.1V, exhibited peak transconductance G_m of 54.1μS and 22.0μS, for SiGe and for poly-Si (L_{poly}=2μm) gates, respectively, demonstrating an improvement to higher G_m in comparison to poly-Si gate.

The threshold-adjust implant doses were selected to allow nominal threshold voltages of ± 0.7V for poly Si gate devices. The same threshold-adjust implant doses were selected for poly Si/SiGe gate devices, so the shift in threshold voltage due to the presence of Ge in the gate material is apparent in the p-MOS and n-MOS device characteristics shown in figures 1 and 2. One can see that, the n-MOS threshold voltage is ≈ + 0.2V and it is suitable for low power n-MOS transistor, RF detector and RFID tag applications. Whereas, the p-MOS threshold voltage is ≈ + 1.0V however, this device has higher G_m than poly Si gate p-MOS as shown figure 1 and 2.

Figures 2 and 3 show the comparison of measured transconductance curves of poly-$Si_{0.7}Ge_{0:3}$ gate MOS transis-

tors for different gate length: L=3, 5, 8, 10 and 20 μm for the same gate width of W=20 μm.

The impact of gate depletion on transistor current drive is estimated by the inversion charge Q_{inv}. As observed by Yu [4], the ratio ($Q_{inv\ SiGe}$ / $Q_{inv\ Si}$) is greater than unit and increases as (V_{GS}-V_T) increases. As shown in figure 1, 2 and 3, this result agrees with the measured G_m curves for poly-$Si_{0:7}Ge_{0:3}$ gate MOS transistors for different gate size.

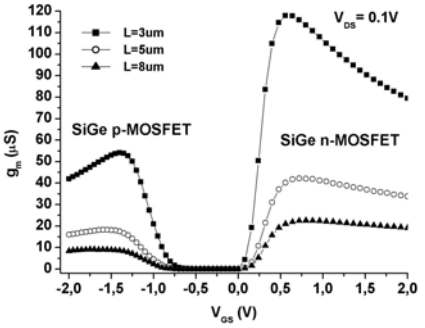

Fig. 2 Plot of G_m with V_{GS} and L=3,5 and 8µm show the shift in threshold voltage

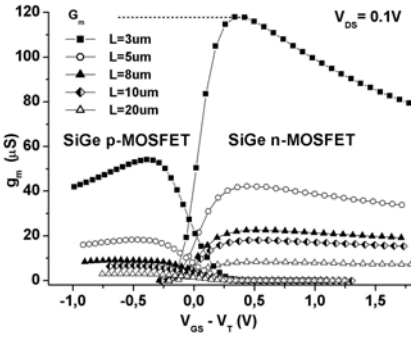

Fig. 3 Plot of G_m with (V_{GS} -V_T) and L=3, 5, 8, 10 and 20µm.

The examination of low-frequency noise (*1/f)* based on the method reported in literature [6], a probe station, a LNA amplifier, a Keitley DC measurement system and a HP 3560A Signal analyzer were used. All data (I_D) is subtracted from amplifier (noise and gain). This result is raised to the square quantified by I_D^2 value, thus one have the Noise Power Spectral Density (drain noise) with dimension (A^2/Hz).

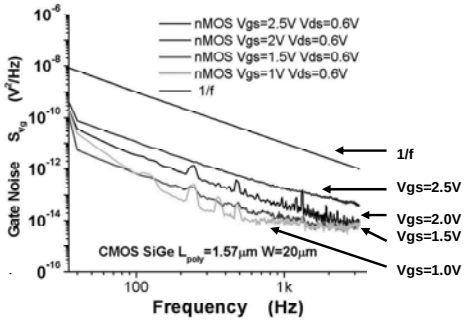

Fig. 4 Plot of Gate Noise S_{Vg} x frequency of n-MOSFET

Figure 4 for n-MOSFET and figure 5 for p-MOSFET shows the plot of Gate Noise Power Spectral Density S_{Vg} x frequency after dividing the data of drain noise by G_m^2 and thus to get S_{Vg}. with the same size L_{poly} =1.57µm, W=20µm and with poly-Si/SiGe gate. The observed results are in agreement with reported noise data in [9], [10]. The gate noise S_{Vg} measurements (for 100Hz noise between 10^{-11} and 10^{-12} for W=20um, L=1,57um) is about the same order presented in literature (for 100Hz, noise between 10^{-11} and 10^{-12} for W=10um, L=0,25um).

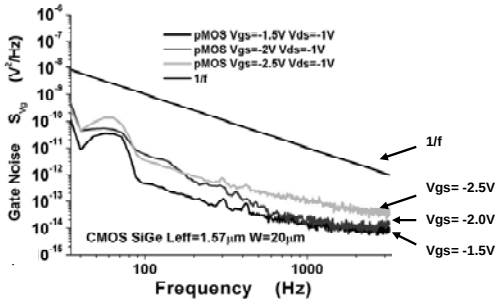

Fig. 5 Plot of Gate Noise S_{Vg} x frequency of: p-MOSFET

3. Conclusions

In summary, a single n^+ doped, poly-$Si_{1-x}Ge_x$ gate CMOS technology is advantageous compared to single n^+ or double doped, poly-Si gate CMOS technology. We had integrated a $Si_{0.7}Ge_{0.3}$ gate material of MOSFET transistors in the CMOS process with few exchanges. We demonstrate a reduction of gate depletion and DC characteristics improvements. The extracted noise values are low and suitable for RF application and these results show a good performance of the fabricated devices.

Acknowledgements

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