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Trap Profile and Bias Temperature Instability of ALD-HfSiON Gate Stacks in Advanced MOSFETs

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1. Introduction

The use of HfSiON as gate dielectric for advanced CMOS technology is attracting much attention due to good mobility of electrons/holes and significant reduction of gate leakage. However, there are critical reliability concerns as trade-offs to its good characteristics for transistors. Nitrogen incorporation in HfSiON was found effective for improving PBTI of nMOS, but unfortunately resulting in poor NBTI lifetime of pMOS and degraded electron/hole mobility. In this work, we simultaneously extract delay-free NBTI over broad range of stress-fields, stress-temperatures and [N]%, model gate leakage current (J_g) and NBTI degradation within a theoretically consistent framework of field-dependent reaction-diffusion (R-D) model, and conclude that the reduction in J_g at NBTI-limited [N]% can be significant and would reduce power dissipation without affecting NBTI-margin. Also, the technique of combining charge pumping method and low frequency noise measurement helps us to monitor the defect distribution in dielectric layers, and support the nitridation mechanism we proposed.

2. Experiments

Figure 1 describes the process flow of HfSiON MOSFETs. Nitridation of the Hf-Silicate films was performed by three different processes using N_2 plasma (N_2-PN), NH_3 plasma (NH_3-PN) and NH_3 thermal (NH_3-TN) nitridation respectively. EOT for the dielectric stack was extracted from measured capacitance-voltage (C-V) characteristics. In addition, X-ray photoelectron spectroscopy (XPS) was carried out to evaluate the chemical bindings and the nitrogen concentration ([N]%) of the prepared HfSiON films. The overall trap distribution within the gate dielectrics is evaluated by combining the results of charge pumping and low frequency noise measurements.

3. Discussions

Figures 2 and 3 show the dependence of I_d-V_g and I_g-V_g characteristics of the HfSiON gate stack devices treated with different nitridation conditions. EOT and [N]% of the gate stacks were found to be 13 Å and around 15%. It reveals that device with N_2-PN exhibits a relatively better subthreshold swing and leakage, which is attributed to a considerable amount of defects inside the HfSiON film has been reduced by N_2 plasma nitridation process.

From the total threshold voltage shift (ΔV_{th}) after the 1000s-1V stress, an activation energy (E_a) was calculated. It reflects the potential energy of the pre-existing electron traps in Hf-Silicate gate dielectric. These traps, which are accessible for direct electron tunneling, can be charged during substrate injection stress, leading to a positive V_{th} shift. Figure 4 shows the V_{th} shift as a linear function of 1/kT. The ΔV_{th} increases with increasing temperature for all HfSiON device samples. The temperature dependence of V_{th} shift is dominated by trapping/diffusion mechanism. ΔV_{th} for PN MOSFETs are smaller than that for TN MOSFETs. The E_a of traps is 0.064eV for PN MOSFETs and 0.0362eV for TN MOSFETs. We found that higher activation energy eases NBTI degradation. The relationship between ΔV_{th} and E_a is found following $\Delta V_{th} \propto \exp(-E_a/KT)$.

Figure 5 shows the time evolution of the BTI of PMOSFETs during stress at room temperature. The semi-log plot indicates that V_{th} shifts due to electron trapping follows a power-law dependence, $\Delta V_{th}=A*t^n$, where t is the stress time, the n value of the PN MOSFETs is about 0.218~0.231, which is commonly observed in typical I_d-V_g measurements [1,2]. ΔV_{th} does depend on different nitridation processes. Negative V_{th} shift during the NBT stress is attributed to the interface trap generation and/or positive oxide charge buildup originating from the dissociation of Si-H bonds at the SiO_2/Si interface, on the basis of a conventional R-D model. The TN Hf-silicate MOSFETs suffer a much higher NBTI than PN ones owing to their Nitridation center which is close to the HfSiON/SiON interface, causing the larger defect precursor (Si-H bond) density and/or lower thermal activation energy to dissociate S-H bonds, both are induced by the nitrogen incorporation. The schematic of interface traps and hole trapping in ALD HfSiON gate stack of the electrochemical reactions occurred during NBTI are shown in Figure 6.

Figures 7 and 8 show the result of conventional charge pumping and low frequency measurements. We found that PN MOSFETs have slightly better interface quality and lower noise density. To further verify the overall defect distribution within the gate dielectric stacks, frequency-dependent charge pumping method can be used for extracting the depth profiles of traps in the SiO_2 interfacial layer [3]. The hold time in accumulation and inversion determines the depth at which traps can contribute to the charge pumping current. Moreover, carrier exchange via tunneling between the inversion layer and the trap sites cause low frequency noise [4]. Applying number fluctuation model of the flicker noise [5], we can calculate the volume

trap density in the HfSiON layer. By combining these two techniques we thoroughly sketch the defect distribution in dielectric stacks, as shown in Figure 9. The result strengthens the conclusion of PN gate dielectric has better film quality due to the trapping center profile is mostly located away from HfSiON/SiON interface.

4. Conclusions

The BTI reliability degradation with HfSiON as gate dielectric was found mainly associated with electron trapping instead of interface states as known in the case of SiON gate dielectric. In this work, the EOT dependence of NBTI in plasma nitridation and thermal nitridation devices is studied using I_d-V_g Extracted ΔV_{th} vs. stress time. A comprehensive study has also been performed to investigate the effect of optimized nitrogen incorporation in HfSiON through defect distribution, EOT, gate leakage, and stress reliability. We conclude that precisely controlled plasma nitridation treatments improve gate dielectric quality, and also reduces J_g and power dissipation significantly without affecting NBTI-margin.

Acknowledgements

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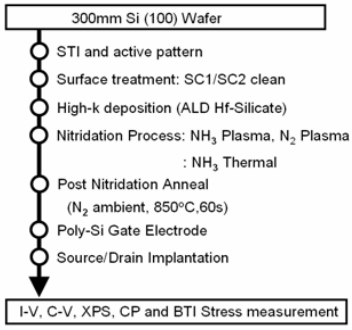

Fig. 1 Fabrication process flow of HfSiON-gated devices.

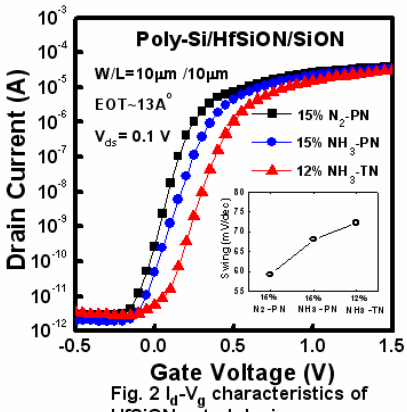

Fig. 2 I_d-V_g characteristics of HfSiON gated devices.

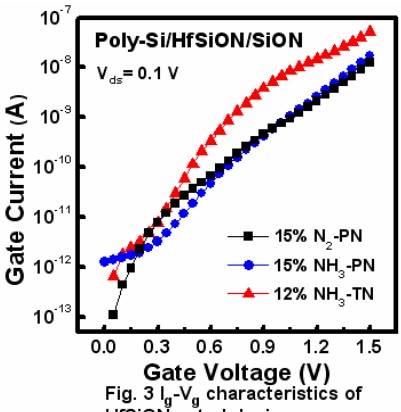

Fig. 3 I_g-V_g characteristics of HfSiON gated devices.

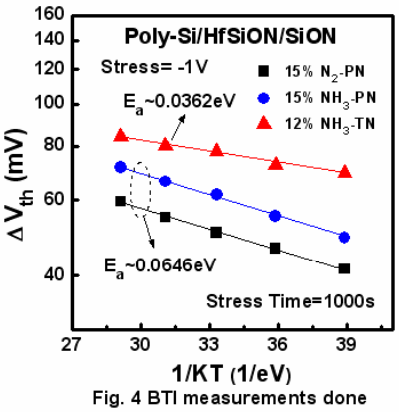

Fig. 4 BTI measurements done at 25°C~125°C.

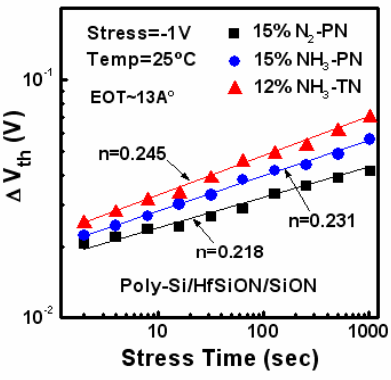

Fig. 5 V_{th} shift of HfSiON pMOSFETs as a function of time.

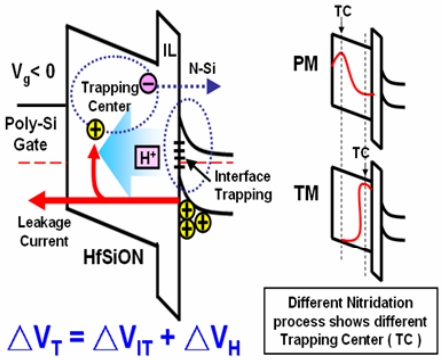

Fig. 6 A schematic of interface traps and hole trapping in ALD HfSiON gate stack of the electrochemical reactions occurred during NBTI.

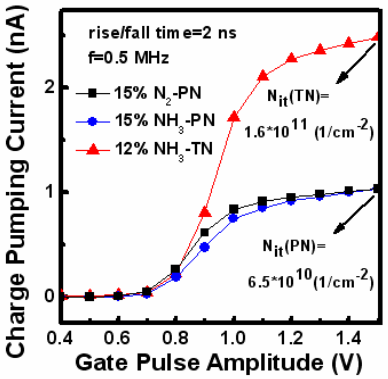

Fig. 7 Charge pumping measurements of HfSiON gated devices.

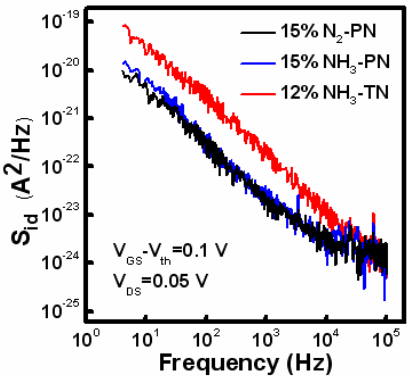

Fig. 8 Low frequency noise measurements of HfSiON gated devices.

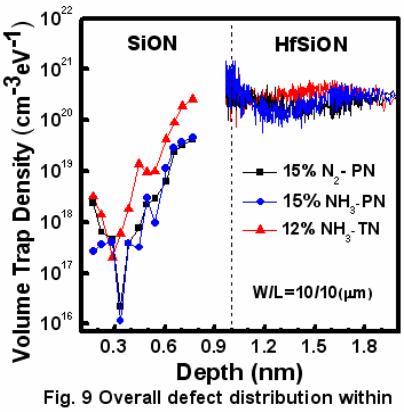

Fig. 9 Overall defect distribution within gate dielectrics.