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Investigation of Novel Si/SiGe Hetero Structures and Gate Induced Source Tunneling for Improvement of P-channel Tunnel FETs

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1. Introduction

Tunnel FET (TFET) with it's sub 60mV/decade is being explored as an alternative for scaled CMOS, especially for low power applications. Whereas a lot of work has been reported on the performance enhancement of the nTFET, relatively few reports have been published on pTFET. Bhuwalka et al. [1] reported the ambipolar working of vertical nTFET with negative gate bias, as a pTFET device. Mayer et al. [2] and Royer et al. [3] has reported SOI, SiGeOI and GeOI pTFET. In all the cases stated above, the ON state current reported for pTFET are about 5uA/um or less. Toh et al. [4] reported a Ge based double gate pTFET with 3nm HfO_2 gate dielectric (very small EOT = 0.46nm) with an ON state current of 1mA/um.

In this paper we have explored the following variations of the simple p-i-n hetro junction pTFET (H-pTFET) architectures shown in Fig. 1 with the aim of improving the pTFET performance: (I) H-pTFET with $Si_{1-\gamma}Ge_{\gamma}$ in the source (II) H-pTFET with $Si_{1-\gamma}Ge_{\gamma}$ source and channel (III) H-pTFET with $Si_{1-\gamma}Ge_{\gamma}$ in the channel (proposed for the first time). It is also shown for the first time that a GIDL like Gate Induced Source Tunneling (GIST) is present in pTFETs and that this effect can be used for further improvements in performance. The 2-D simulations were performed using Synopsis TCAD tool, MEDICI [5]. Kane model for tunneling is used with default parameters which has been reported to reproduce experimental data [6].

2. Optimization of pTFET

A. Effect of Germanium Mole Fraction

Fig. 2 shows the I_D-V_{GS} characteristics for structure I. As the γ is increased from 0 to 0.2, it is seen that the I_D-V_{GS} for the later case follows the former upto a V_{GS} of about -0.67V, and at -0.67V, there is an inflection in the curve and the subthreshold swing increases abruptly. As γ is increased further the inflection point shifts to the right and for γ=0.5, the inflection point is not identifiable. As seen from Fig. 3 at low V_{GS}, before the inflection point, electron tunneling is from the valance band (VB) in the channel to the conduction band (CB) in the source in both the cases (γ=0 and γ=0.3) leading to similar I_D-V_{GS} trends. However, as V_{GS} is increased, in the case of the H-pTFET, electron tunneling can happen from VB at the edge of the source SiGe to CB in the source itself, resulting in an abrupt change in the I_D-V_{GS} behavior. To optimize ON currents, the workfunction(WF) can be increased for low γ values, so that the I_D-V_{GS} is shifted to the right thereby increasing the ON current or the gate WF is held constant at 5.27eV and γ is optimized for a given supply voltage. For example, for a V_{DD} = 1V, the optimum value of γ is 0.3 for the structure I.

We also observed a decrease in the transconductance as the γ is increased. This is explained by the band diagrams shown in Fig. 4. It is seen that for large gate voltages, the tunnel width in the source increases with increasing γ leading to lower ON state current.

B. Gate Induced Source Tunneling (GIST)

As the Gate to source overlap is varied from 2 to 8nm, the ON current tends to improve as seen from the I_D-V_{GS} characteristics(Fig. 5). It is seen that the peak electric field (Fig. 6), seen at the Si-SiGe junction, decreases as the overlap length is increased but the breath of the second peak increases with increasing gate-source overlap. The vertical tunneling width seen in Fig. 7 is less than the lateral tunnel width seen in Fig. 4, for identical bias conditions. The vertical tunneling happens in a broader region as the overlap length is increased as indicated in Fig. 6, resulting in an increase in I_D with increasing overlap length.

C. Impact of Device Architecture

The performance of the three hetero structure architectures are compared in Fig. 8. Structure I (SiGe source) has superior sub-threshold slope compared to the other two structures. However structure I has higher threshold voltage and lower ON state current for a V_{DD} of 1V. The best ON state current and low threshold voltage are obtained for structure III (SiGe in the channel). OFF state current is seen to be independent of device architecture for the three variants investigated.

3. Conclusions

All the three hetero structures investigated are predicted to give better ON state currents than previously reported devices as indicated in Table I except Ge TFET reported by Toh et al. [4], (EOT=0.47nm). The newly proposed structure III with $Si_{0.66}Ge_{0.34}$ channel is seen to give the best ON state current which is about 42 times better than the comparable devices reported in the literature. Interband tunneling (both lateral and gate induced vertical components) in the source region are found to contribute significantly to the current conduction.

References

[1] K.K Bhuwalka et al. Jpn. J. Appl. Phys. **45** (2006) 3106.
[2] F. Mayer et al. Tech. Dig. IEDM (2008) 163.
[3] C. Royer et al. Tech. Dig. ULIS (2009) 53.
[4] E. H. Toh et al Jpn. J. Appl. Phys. **39** (2008) 104504-1.
[5] Synopsys TCAD Design Suite. http://www.synopsys.com
[6] K.K Bhuwalka et al. IEEE Tran. Elec. Dev. **52** (2005) 924

TABLE I
COMPARISON OF DIFFERENT P-CHANNEL TFETS REPORTED IN THIS WORK AND THE LITERATURE.

Ref	p-i-n structure	Exp. (E) Sim. (S)	Channel length (nm)	Ge mole fraction	EOT (nm)	$\|V_{DS}\|$ (V)	$\|V_{GS}\|$ (V)	I_{on} (μA/μm)	I_{off} (fA/μm)	SS (mV/dec
This Work	SiGe source	S	20	0.3	1	1	1	5.6	0.62	16.73
	SiGe source & channel	S	20	0.36	1	1	1	22.6	1.5	50.1
	SiGe channel	S	20	0.34	1	1	1	42.1	19.6	44.59
[1]	Vertical Si TFET	E	25	–	4.5	0.7	4.5	1	10000	>100
[4]	Double Gate Ge TFET	S	50	0.2	0.47	1.2	1.2	1000	1	12.3
[2][3]	Ge TFET	E	300	–	–	0.8	2	3	1e7	>100

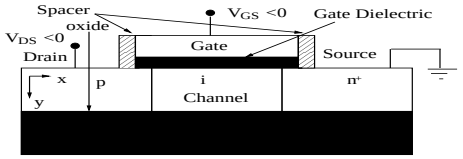

Fig. 1. The p-i-n pTFET structure with the bias conditions used in this work. Gate dielectric is 1nm oxide, workfunction (WF) is 5.27 eV, SOI thickness is 50nm and the channel length is fixed to 20nm.

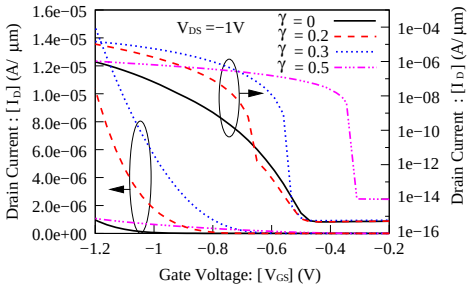

Fig. 2. I_D-V_{GS} Characteristics of HTFET (structure I, with $Si_{1-\gamma}Ge_{\gamma}$ source) with variation in Ge mole fraction.

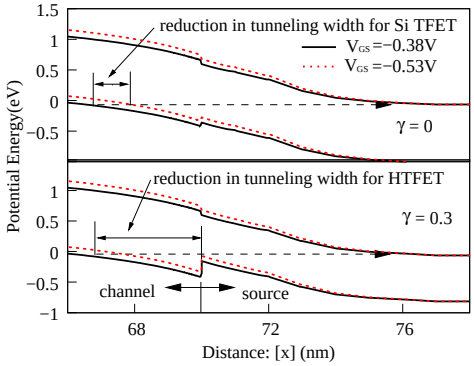

Fig. 3. Band diagram along the channel length for p-channel (a) Silicon TFET (top) and (b) hetero junction TFET (bottom), at low gate voltages. V_{DS} = -1V.

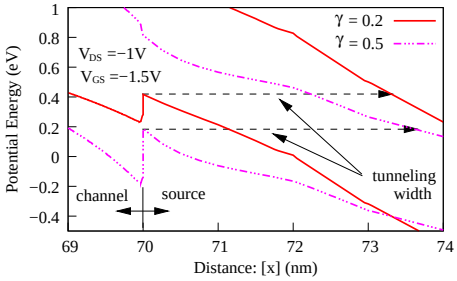

Fig. 4. Band diagram along the channel length for increasing γ for large gate voltage. The tunneling width is larger for γ=0.5 as compared to γ=0.2.

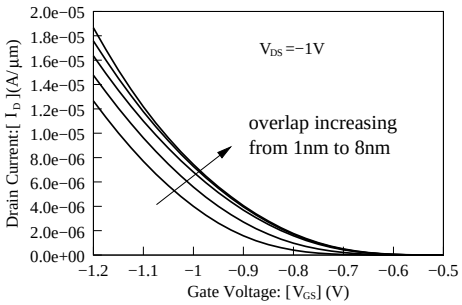

Fig. 5. I_D increases with increasing gate to source overlap for Structure I with $Si_{0.7}Ge_{0.3}$ source. V_{GS} = -1.5V, V_{DS} = -1V.

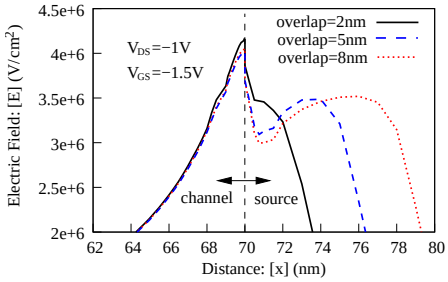

Fig. 6. Total electric field in Structure I with $Si_{0.7}Ge_{0.3}$ source along the channel length for gate-source overlap lengths of 2, 5 and 8nm.

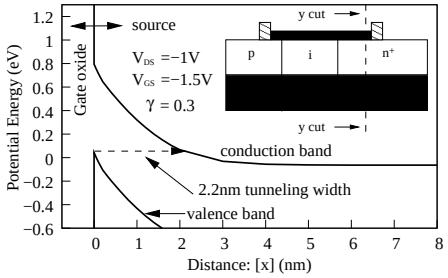

Fig. 7. Band bending along a vertical cut line through the gate and source.

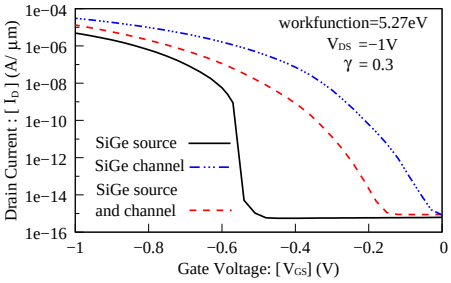

Fig. 8. Transfer characteristic for p-channel HTFET with (I) SiGe source (II) SiGe source and channel (III) SiGe channel. γ=0.3 and gate-source overlap is 2nm.