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Recovery of CHC- and NBTI-induced Degradation on MOSFETs by Using Different Annealing Treatments

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1. Introduction

Through the continuous shrinking of transistor dimensions, the channel hot-carrier (CHC) and negative bias temperature instability (NBTI) effects on MOSFETs are both the most critical reliability issues that may eventually determine the lifetime of the CMOS devices. It is well-known that MOSFET properties after CHC and NBTI degrade due to the increment of oxide trapped charges (N_{ot}) and interface states (N_{it}).

Some researches thought that CHC-induced the degradation is due to the breaking of Si-H bonds to increase N_{it} and N_{ot} [1-3]. After, the researches reported that hole trapping is dominant for NBTI-induced device degradation and recovery effect is inferred to N_{ot} improvement, but N_{it} recovery is very slight [4-5]. Most of the researches followed Reaction-Diffusion model (R-D model) and confirmed that the released H species is due to the breaking of Si-H bonds to induce N_{ot} or N_{it} and is a critical mechanism [6-7]. The cause is supposed that the Si-H bonding force is very weak to easily make Si dangling bond and the released H species may diffuse into gate dielectric to create more N_{ot}. A latest study reported that NBTI-degraded MOSFET properties can be entirely recovered at 325 ℃ with bake [8]. However, this study unclearly explained the true mechanism of degradation or recovery effect. The degradation or recovery effects of MOSFET properties seem not entirely assure to come from the variation of the broken Si-H bonds. So, it is quite important to find the true mechanism from the foregoing reliability issues.

In this study, try to find the main mechanism is our motivation after CHC or NBTI. With the different annealing treatments, the variations of threshold voltage (V_t), saturation current (I_{dsat}), and transconductance (g_m) of MOSFETs were showed. Furthermore, by using subthreshold swing method, the variation of N_{it} (ΔN_{it}) clearly showed the recovery effect after CHC and NBTI.

2. Experiment and result discussions

All tested devices were fabricated using 0.18 μm process of United Microelectronics Corporation (UMC). The gate dielectric is SiO_2 and gate oxide thickness (T_{ox}) is 32 Å. MOSFETs' properties after CHC and NBTI are extracted at different measurement time, including Fresh, Stress, Anneal after stress, and Still. The annealing treatments are 100 % N_2 and 95 % N_2 + 5 % H_2 respectively. Annealing condition was performed at 400 ℃ for 30 minutes. Fig. 1 briefly shows the procedures of this work.

Figure 2 shows that V_t shifts after pMOSFET at NBTI and nMOSFET at CHC and the exponents of n are about 0.23 and 0.35. The degradation increased after CHC and NBTI is a result of the breaking of Si-H bonds at the interface of SiO_2/Si-bulk (bottom interface) and n value depends on the one-dimension (for NBTI) or two-dimension (for CHC) diffusion of hydrogen [2-3]. Fig. 3 shows I_{dsat} degradation after CHC and NBTI stress. The trend of I_{dsat} degradation on nMOSFETs is similar to V_t shift of Fig. 2 at CHC mode. The results show that temperature factor is apparently correlated with NBTI, but stress voltage is not.

Figure 4 shows the I_{dsat}-V_g characteristics of fresh MOSFETs with and without annealing, which shows the annealing treatment did not change the properties of unstressed devices.

Figures 5 and 6 show that CHC recovery is observed in nMOSFET under the different annealing treatments. "Still" indicates that the data after CHC is measured 14 days later and less recovery is observed. Recovery ratio ($R_{recovery}$) is calculated with the recovery amount of Fresh-Stress over the recovery amount of Anneal-Stress. It is separately about 91 % in 100 % N_2 annealing and 96 % in 95 % N_2 + 5 % H_2 annealing. On the other hand, Figs 7 and 8 show the similar results. In pMOSFET, NBTI $R_{recovery}$ is respectively about 131 % in 100 % N_2 annealing and 137 % in 95 % N_2 + 5 % H_2 annealing. From Figs 5 to 8, it is found that the recovery of CHC in nMOSFET or NBTI in pMOSFET is strongly correlated with temperature, but is independent of N_2 or H_2 incorporation. The recovery variation of MOSFETs' properties is small in two annealing treatments.

Figure 9 shows the comparisons of g_m-V_g characteristics at the said annealing treatments. Separately, CHC $R_{recovery}$ is about 105 % in 100 % N_2 annealing and 98 % in 95 % N_2 + 5 % H_2 annealing. In Fig. 10, NBTI $R_{recovery}$ is about 101 % in 100 % N_2 annealing and 128 % in 95 % N_2 + 5 % H_2 annealing. The g_m characteristic is correlated with the variation of N_{it} at the bottom interface. N_{it} seems to be easily recovered by using high temperature annealing.

By subthreshold swing method, Figs. 11 and 12 reveal that the large recoveries of ΔN_{it} after annealing are apparently observed at CHC in nMOSFET or at NBTI in pMOSFET. The variation is so slight for the recovery of ΔN_{ot}. The results are contrary to the viewpoint of the popular R-D model [6-7]. We suppose that the high temperature should induce the released H species more diffuse away, but ΔN_{it} almost completely recovers. So, the cause may be due to H species staying near the broken bonds at the bottom interface. Furthermore, as for the slope (n value) variations of degradation (e.g. V_{th} shift), they may be only due to different bonding energy resulted from strained bonding.

3. Conclusions

In this work, it is observed that stress-induced MOSFET degradation is recovered under high temperature annealing. The results prove that ΔN_{it} can be recovered and dominates the improvement of MOSFET characteristics. ΔN_{ot} recovery is also observed but only possesses small portion in our experiments. Thus, the recovery of large quaintly ΔN_{it} after annealing is conjectured to be due to most of the released H species staying near the interface of SiO_2/Si-bulk. Therefore, it is suggested that the contents of Reaction-Diffusion model should be reexamined.

References

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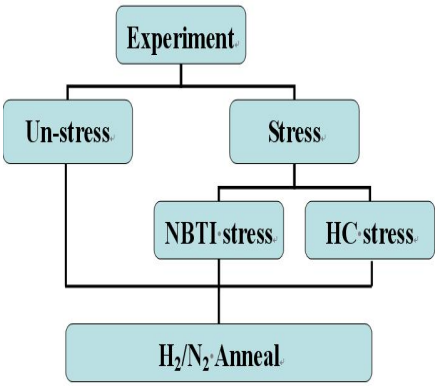

Fig. 1. The annealing experimental procedures with and without stress.

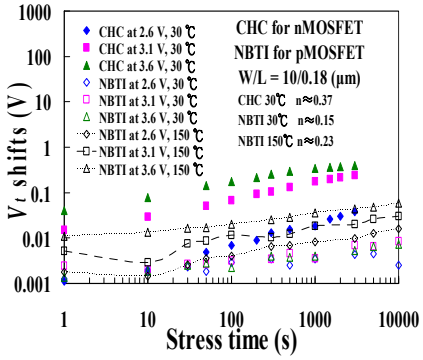

Fig. 2. In log-log scale, V_t shifts of MOSFETs after CHC and NBTI are illustrated

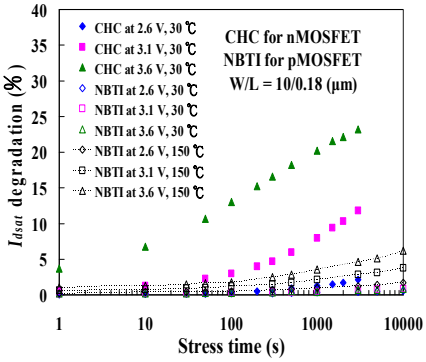

Fig. 3. The I_{dsat} degradation of MOSFETs after CHC and NBTI stress.

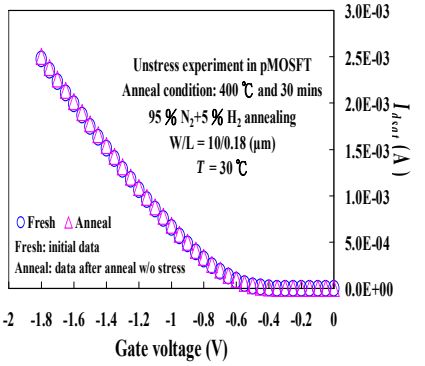

Fig. 4. The unstress I_d-V_g curves are measured with and without annealing.

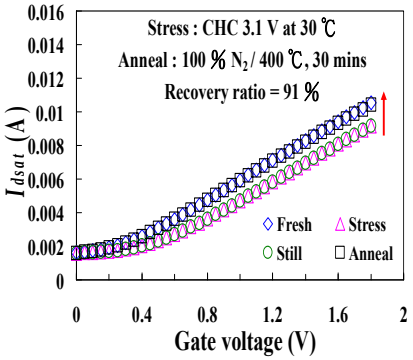

Fig. 5. CHC recovery in nMOSFET after 100% N_2 annealing.

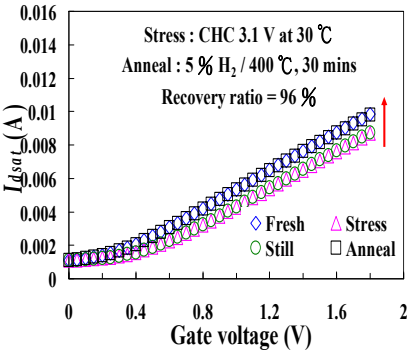

Fig. 6. CHC recovery in nMOSFET after 95 % N_2+5 % H_2 annealing.

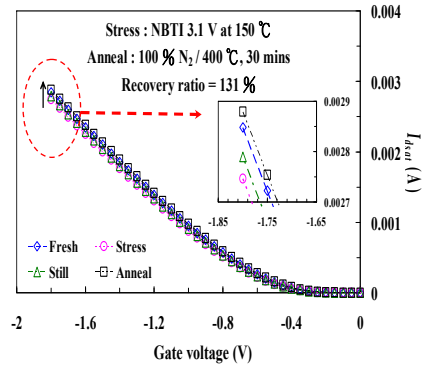

Fig. 7. NBTI recovery in pMOSFET after 100 % N_2 annealing.

Fig. 8. NBTI recovery in pMOSFET after 95 % N_2+5 % H_2 annealing.

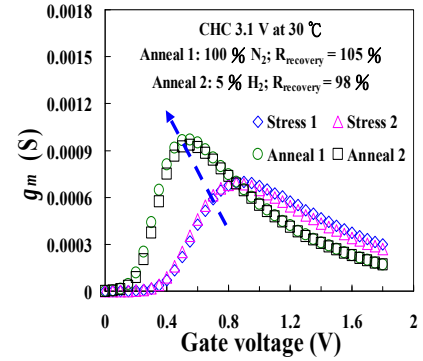

Fig. 9. nMOSFET g_m curves after CHC are plotted in various annealing treatments.

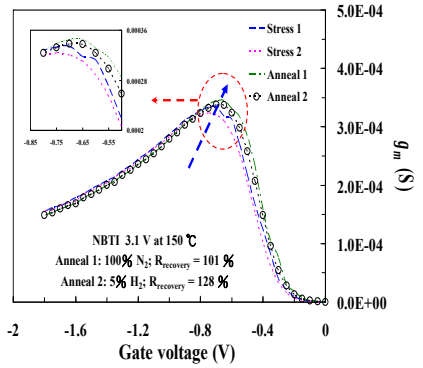

Fig. 10. pMOSFET g_m curves after NBTI in various annealing treatments.

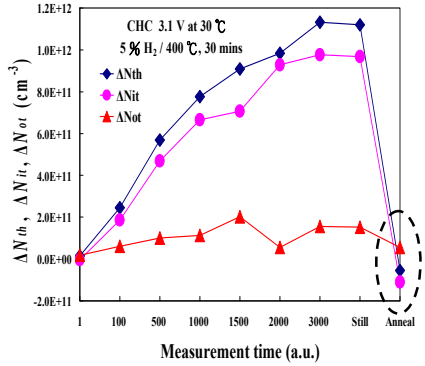

Fig. 11. Defect recovery after CHC in different measurement time.

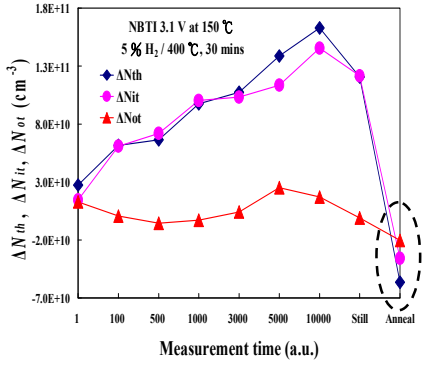

Fig. 12. Defect recovery after NBTI n different measurement time.