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Ultra thin Ni-silicides with low contact resistance on SOI and strained-SOI

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Abstract: Ultra thin Ni-silicides are formed on both SOI and biaxially strained Si-on-insulator (SSOI) substrates. With a thin Ni layer of <4nm, a high quality epitaxial $NiSi_2$ layer was grown at a low temperature of 500°C. A very thin Pt interlayer to incorporate Pt to NiSi improves the thermal stability, the interface roughness and lowers the contact resistance. The contact resistivity of the epi-$NiSi_2$ on SOI is about one order of magnitude lower than that of a NiSi layer, and 5.5 times lower than $Ni_{1-x}Pt_xSi$.

1. Introduction

As the dimensions of devices are scaled down, the silicide layer that is used as source/drain contacts should be very thin, especially for SOI devices in order to achieve low series resistance [1]. Among silicides, NiSi is the most suitable material for nanometer devices. However, its low thermal stability and polycrystalline phase lead to a rough interface. Platinum (Pt)-incorporation into Ni-silicide to form $Ni_{1-x}Pt_xSi$ improves the thermal stability, and lowers the contact resistivity [2,3]. The grain size of $Ni_{1-x}Pt_xSi$ is smaller, making the interface smoother than for pure NiSi [3]. Another approach to improve the thermal stability and interface roughness is to employ epitaxial silicides. Nickel disilicide ($NiSi_2$) is one of the promising candidate materials since it has a very small lattice mismatch of -0.4% with respect to Si. Epitaxial $NiSi_2$ layers on Si(001) can be easily formed by solid-phase reaction of Ni with Si at temperatures >700°C. However, $NiSi_2$ layers often exhibit a discontinuous and inhomogeneous morphology induced by the inhomogeneous formation of {111} facets at the $NiSi_2$/Si(100) interface.

For the first time, ultra-thin epi-$NiSi_2$ and $Ni_{1-x}Pt_xSi$ layers are investigated on both, SOI and high mobility strained Si-on-insulator (SSOI. As a result, epitaxial-pi-$NiSi_2$ shows a much lower contact resistivity than $Ni_{1-x}Pt_xSi$ and NiSi.

2. Ultra thin silicide formation

Intrinsic SOI (100) and SSOI (100) wafers with a respective top Si thickness of 88nm and a strained Si layer of 70nm were used as starting materials. The thickness of the buried oxide (BOX) for both SOI and SSOI is 145nm. In this experiment SSOI with a biaxial tensile strain of ε_{biax} = 0.8%, corresponding to a stress of 1.3 GPa was used. After cleaning and HF-dip to remove the thin oxide on the surface, Ni layers with thicknesses of 3 nm and 5nm were deposited, respectively. For the Pt-incorporation Ni silicide, a Pt layer with a thickness of <1nm was deposited prior to Ni deposition. Then the samples were annealed by RTP at different temperatures for 10s in forming gas (90% N_2+ 10% H_2) to form silicides. The residual unreacted metal was chemically etched selectively. Fig.1 shows the thermal stability of the silicide layers formed on SOI by plotting the sheet resistance R_s of the silicide layer as a function of the RTP temperature. For the 3nm Ni layer, the sheet resistance of the as-formed silicide layer decreases with increasing temperature. The layer is stable up to 900°C. We will show that an epitaxial $NiSi_2$ layer with a thickness of ~10nm is formed at RTP temperatures >500°C. At 850°C, a sheet resistance of 41 Ω/square, corresponding to a specific resistivity of ~45 Ωcm, was obtained for the epi-$NiSi_2$ layer. However, no epi $NiSi_2$ layer was formed when a thin Pt interlayer was deposited prior to 3nm Ni deposition. The $Ni_{1-x}Pt_xSi$ layer shows a low sheet resistance in a temperature window from 400 to 500°C, as indicated in Fig.1(a). Fig1(b) shows the silicides formed with 5nm Ni with and without Pt interlayer. Monosilide layers were formed with low sheet resistance. Pt-incorporation into the silicide increases the thermal stability from 600 to 700°C. The minimum sheet resistance amounts to 15 Ω/square for NiSi and 30 Ω/square for $Ni_{1-x}Pt_xSi$, respectively

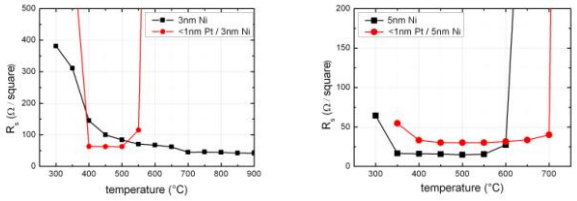

Fig.1 Thermal stability of Ni-silicides with different thicknesses formed on SOI. With 3nm Ni epi- $NiSi_2$ was formed at –T >500°C.

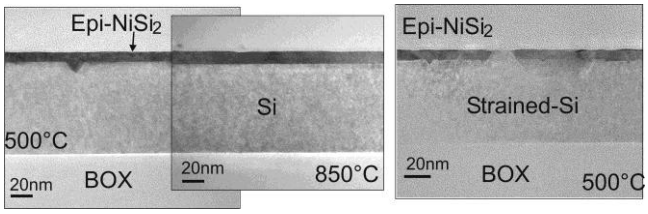

Fig.2. Cross section TEM showing epi-$NiSi_2$ layers formed on both SOI and sSOI with 3nm Ni.

Fig.2 shows the cross section TEM images of epi-$NiSi_2$ formed with 3nm Ni on both, SOI and SSOI at 500°C and 850°C, respectively. XRD and RBS/channeling measurements proved that the $NiSi_2$ layer is epitaxially grown at temperatures > 500°C (not shown). The $NiSi_2$ layer formed at 500°C is very uniform except for a few pyramids

with wedge-shaped (111) facets at the interface. Silicidation at 850°C results in a much better interface. No pyramids were observed at the interface. The layer thickness increases from 9 nm at 500°C to 11 nm at 850°C. However, on SSOI pinholes and defects are found in the $NiSi_2$ layer due to the tensile strain. On biaxially tensile strained SSOI a larger strain would be created in $NiSi_2$ layer because the lattice constant of $NiSi_2$ is even 0.4% smaller than that of unstrained Si.

Fig.3 shows the cross section TEM images of the silicide layers formed using 5nm Ni with and without Pt interlayer on both SOI and SSOI at 500°C. The layers are very uniform with a thickness of ~11 nm. The $Ni_{1-x}Pt_xSi$ layers formed on both, SOI and SSOI show a smoother interface to the underlying SOI and SSOI layers than NiSi. The strain in the SSOI layer does not influence the silicide formation at 500°C.

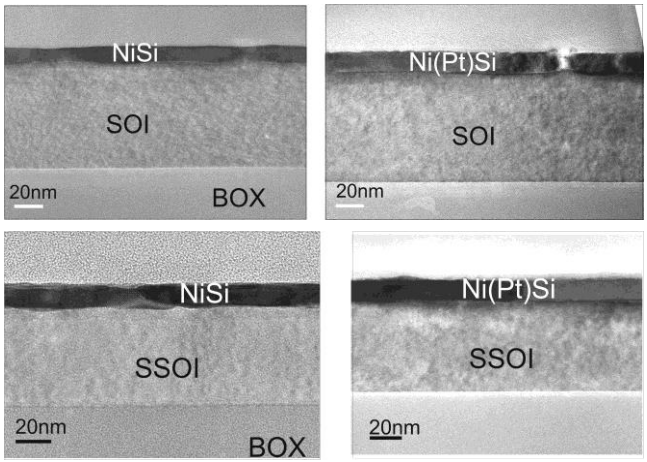

Fig.3 XTEM images of NiSi and $Ni_{1-x}Pt_xSi$ formed on both SOI and SSOI at 500°C for 10s.

3. Contact resistance

The contact resistance was measured using transmission line model (TLM) structure. SOI and SSOI substrates were first implanted with As^+ at an energy of 30keV to a dose of 2×10^{15} cm^{-2}. Then the implanted samples were annealed at 1000°C for 1min to activate the implanted dopants. After patterning an oxide layer deposited by LPCVD, silicidation was performed to form the TLM structure. Finally, Al contacts were deposited on the silicide pads. Fig.4 shows the SIMS profiles after silicidation at 500°C with 1nm Pt/ 5nm Ni on SOI. The arrow in Fig.4 indicates the silicide/Si interface. We can see that Pt atoms show similar profile as Ni. The implanted As atoms segregate at the silicide/Si interface, indicated by the small peak of As at the interface.

The contact resistance and the sheet resistance of the Si layer were extracted from the TLM measurements. For the non-uniformly doped SOI layer as indicated by Fig.4, the sheet resistance of the Si layer is extracted to be 130Ω/square. The contact resistivity R_c values for silicides formed at 500°C are summarized in Fig.5. We can see that the epi-$NiSi_2$ layer formed on SOI shows the lowest contact resistivity, surprisingly 7 and 5.5 times lower than for NiSi and $Ni_{1-x}Pt_xSi$ on SOI, respectively. Comparing $Ni_{1-x}Pt_xSi$ and NiSi indicates a lower contact resistance for $Ni_{1-x}Pt_xSi$ on both SOI and SSOI, in agreement with Ref.[3]. Interestingly, on SSOI $Ni_{1-x}Pt_xSi$ shows a smaller contact resistance than on SOI.

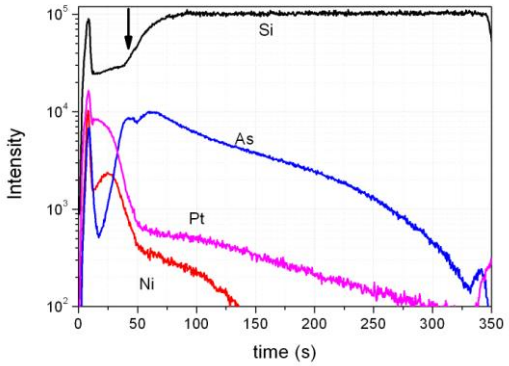

Fig.4 SIMS profiles of $Ni_{1-x}Pt_xSi$ formed on As implanted and subsequently annealed SOI substrates.

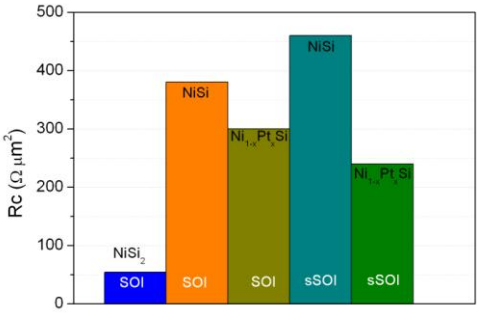

Fig.5. Contact resistance of various Ni-silicides on SOI and SSOI.

4. Conclusions

The formation and contact resistance of ultra thin silicides on SOI and SSOI have been investigated. High quality epi-$NiSi_2$ layers have been achieved by annealing a thin Ni layer (<4nm) at >500°C. Layers with Pt-incorporated into NiSi showed a higher thermal stability, better interface and lower contact resistance on both. As major results, epi-$NiSi_2$ layer formed on SOI shows the lowest contact resistivity, about one order of magnitude smaller than NiSi.

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References

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