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Experimental Analysis of Anisotropic Impact Ionization in (110) Surface pMOSFETs

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1. Introduction

The use of (110) surface orientation has attracted considerable attention for boosting pMOSFETs performance owing to higher hole mobility [1]. However, the (110) surface pMOSFETs have to be located on the same direction, i.e. the layout limitation, due to the anisotropic hole mobility on the (110) surface [2]. This is because the hole mobility shows to be a significant degradation when the channel direction is rotated from <110> to <100> direction on (110) surface pMOSFETs, as shown in Fig. 1. In addition, it has been reported that the substrate current caused by the impact ionization process is dependent on the current flow direction and the impact ionization efficiency (IIE) also appears to be anisotropic [3],[4]. To our knowledge, the physical mechanism of anisotropic IIE in (110) surface pMOSFETs has not yet been fully understood.

The aim of this paper is to focus on the experimental analysis of anisotropic IIE in (110) surface pMOSFETs. From the relationship between the IIE and the electric field in the pinch-off region, the present understanding of anisotropic IIE can be substantially improved.

2. Experimental

The pMOSFETs used in this study were fabricated on a (110) surface Si substrate based on a 90nm CMOS technology. To focus on the effect of the surface orientation on the drain current (I_D) and the IIE, we have to minimize CMOS process-induced strain into the device channel. For example, the space of the gate edge to shallow trench isolation sidewall is chosen to be 5 um. For comparison, a control-Si device was also fabricated on a (100) surface Si substrate by using the same CMOS process. Here, two gate dimensions (W/L) of 10um/1um and 10um/0.1um are termed as a long-channel and a short-channel pMOSFETs, respectively.

3. Results and Discussion

Figure 2 shows the (110) surface orientation induced I_D enhancement ratio of 58% for <110> and 35% for <100> direction on the long-channel pMOSFETs relative to the (100) surface control-Si. For the short-channel (110) surface pMOSFETs, two I_D enhancement ratios of 45% for <110> and 32% for <100> direction are shown in Fig. 3. It has been noted that the difference in I_D enhancement between the <110> and the <100> direction on (110) surface pMOSFETs becomes smaller with reduced the channel length. This result of I_D enhancement appears to be similar to the value reported in Ref. [5],[6]. In addition, through the source terminal floating technique [7], the excess diode leakage current even at the large drain voltage (V_D) has markedly smaller effect on the substrate current (I_B) caused by impact ionization process (not shown here). Thus, the impact ionization multiplication coefficient M-1 as a function of V_D is approximately the ratio of the I_B to I_D, that is, M-1(V_D)≈I_B/I_D. Due to the I_B associated with the maximum electric field E_m near the drain, it is necessary to translate M-1(V_D) into M-1(E_m). According to the lucky electron model [8], M-1(E_m) is described as

$$\text{M-1} \approx \frac{I_B}{I_D} \propto E_m \exp\left(\frac{-\varphi_i}{q\lambda E_m}\right), \quad (1)$$

where φ_i is the threshold energy for impact ionization and λ is the mean free path. Moreover, E_m can be expressed as

$$E_m = \frac{V_D - V_{dsat}}{l}, \quad (2)$$

where V_{dsat} is the voltage at the pinch-off point and l is the effective pinch-off length. E_m in Eq. (2) can be indirectly assessed through V_D-V_{dsat}. As predicted by Eqs. (1) and (2), the slope of the $\ln[I_B/I_D(V_D\text{-}V_{dsat})]$ versus $1/(V_D\text{-}V_{dsat})$ plot is represented by $-\varphi_i l/\lambda$. To differentiate between the contribution of these components (l, λ, and φ_i) to the IIE, a comparison of the slope change between the <110> and <100> directions on (110) surface pMOSFETs is made, as shown in Fig. 4. First, the l contribution to the IIE measured on the same (110) surface pMOSFETs with the long channel L of 1um is reasonably assumed to be negligible. Then, a constant high gate voltage of 3.2V is adopted to stress the gate oxide, with source, drain, and substrate tied to ground. The subthreshold characteristics and the low-voltage tunneling current show an increase in the SiO_2/Si interface traps density, as shown in Fig. 5 and Fig. 6, and provide another condition for the modulation of the mean free path, λ. Relative to fresh device, the slope of a high-voltage stressing device appears to be consistent as shown in Fig. 4, implying that the surface orientation dependence of IIE can be attributed to the anisotropic threshold energy, φ_i. Similarly, the slope plot is made for the short-channel (110) pMOSFETs taking into account the series resistance of drain region ($V_D{*}=V_D\text{-}I_DR_D$; $V_{dsat}{*}=V_{dsat}\text{-}I_DR_D$), as shown in Fig. 7. Finally, the difference in slope change between <110> and <100> directions becomes smaller as decreasing the channel length, and the slope of a high-voltage stressing device appears to be inconsistent with that of fresh device. This result could be explained by the cause of non-stationary transport [9].

4. Conclusions

Experimental analysis of anisotropic IIE in (110) surface pMOSFETs has been presented. From the relationship between the IIE and the E_m, the surface orientation dependence of IIE can be reasonably attributed to the anisotropic threshold energy,

φ_i , regardless of the change of the mean free path, λ . As for the short-channel (110) surface pMOSFETs, the anisotropic IIE becomes smaller and it could be explained by the cause of non-stationary transport.

Reference

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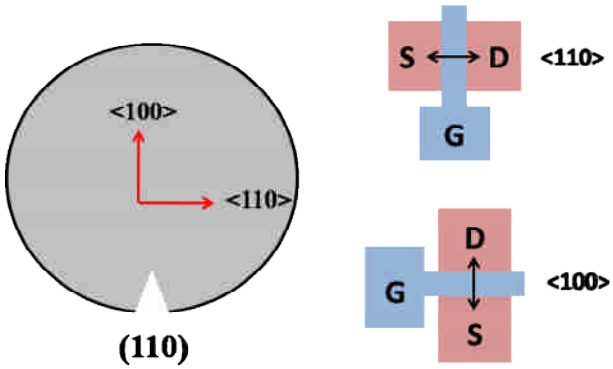

Fig. 1 Schematic illustration of (110) surface pMOSFETs with two channel directions, i.e. <110> and <100>.

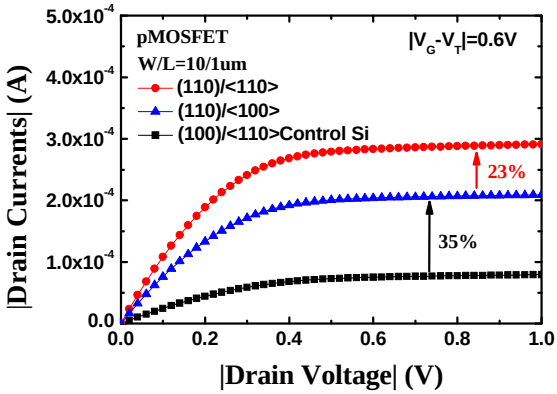

Fig. 2 I_D-V_D characteristics of (110) surface pMOSFETs with a long channel (L=1um) relative to control-Si device.

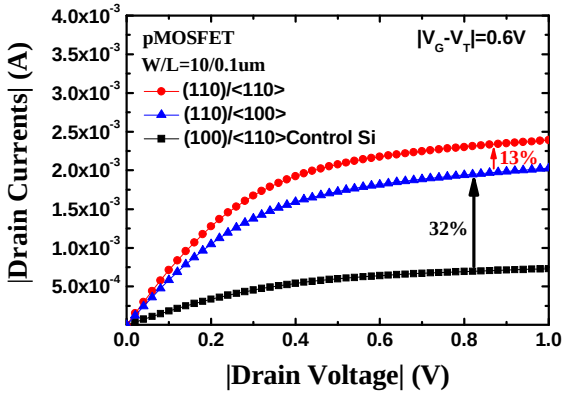

Fig. 3 I_D-V_D characteristics of (110) surface pMOSFETs with a short channel (L=0.1um) relative to control-Si device.

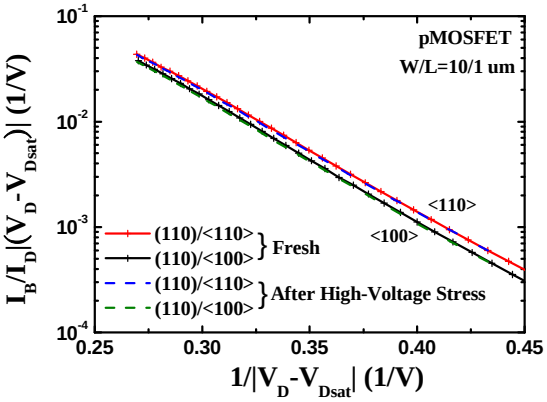

Fig. 4 $1/|V_D\text{-}V_{dsat}|$ dependence of I_B/I_D $|V_D\text{-}V_{dsat}|$ for <110> and <100> direction on a long-channel (110) surface pMOSFETs. The result of pMOSFETs undergoing the high-voltage stress is also shown for comparison.

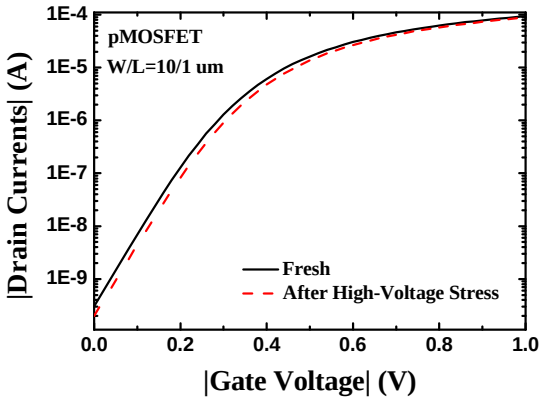

Fig. 5 Subthreshold characteristics of a long-channel (110) surface pMOSFETs before and after the high-voltage stress.

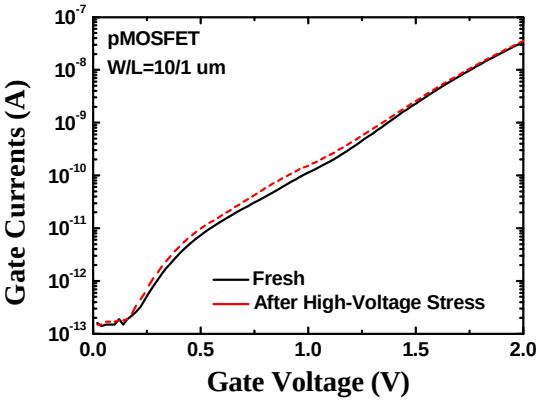

Fig. 6 Gate currents of a long-channel (110) surface pMOSFETs measured in accumulation region before and after the high-voltage stress.

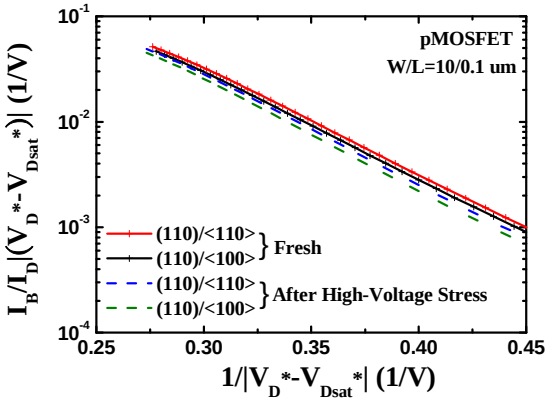

Fig. 7 $1/|V_D\text{-}V_{dsat}|$ dependence of I_B/I_D $|V_D\text{-}V_{dsat}|$ for <110> and <100> direction on a short-channel (110) surface pMOSFETs. The result of pMOSFETs undergoing the high-voltage stress is also shown for comparison.