A Novel Capacitor-less 1T-DRAM on Partially Depleted SOI pMOSFET Based on Direct-tunneling Current in the Partial n+ Poly Gate

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1. Introduction

For both scaling consideration and low process cost, floating body cells of Partially Depleted (PD) SOI seem to be a promising candidate for the new generation of embedded DRAM. This new memory concept is based on charging the body with the majority carriers generated either by impact ionization [1], gate-induced drain leakage (GIDL) current [2] or intrinsic bipolar [3]. In this paper, we propose for the first time, a new 1T-DRAM cell using a pMOSFET with a partial n+ poly-gate on PDSOI and a thin gate oxide. In this case, the excess of majority carriers in the floating body is induced by the direct-tunneling current from the partial n+ poly-gate of the pMOSFET into the n type silicon substrate through the thin gate oxide. For evaluating the validity of this new 1T-DRAM concept, the basic memory characteristics such as read current margin, retention time have been performed. Furthermore, this new concept of capacitor-less 1T-DRAM exhibits very low power consumption during the write "1" operation.

2. Mechanism of Memory Operation with ECB Tunneling Current and Memory Cell Characteristics

PD-SOI MOSFETs were fabricated in STMicroelectronics on conventional 300 mm Unibond® wafers with a 1.6 nm physical gate oxide, a 70 nm silicon film and a 145nm buried oxide. SOI MOSFETs were generally designed with two kinds of layout: 3-terminals for no body tied devices, or Body Contacted (BC) devices with body tied. In this paper, the body contact of BC pMOSFET is voluntarily left floating in order to study the transient effects for 1T-DRAM applications. The lateral poly-gate of BC pMOSFETs is partially covered by n+ implant to form the extra body terminal (Fig. 1). Therefore, the body contact of pMOSFET is defined by the following stack: n+ poly-gate, thin gate oxide and n type silicon film. The main direct tunneling currents in a PD BC pMOSFET under strong inversion are illustrated in Fig. 2. EVB and HVB tunneling currents are respectively the electron tunneling from p+ poly-gate into the silicon substrate and the hole tunneling from the valence band of the n type silicon substrate to the p+ poly gate. The ECB tunneling from the partial n+ poly-Si gate of BC pMOSFET is the dominant mechanism because the barrier height for the electrons in the n+ poly-gate is only 3.1 eV and electron density is high.

The main consequences of this ECB tunneling current in terms of pMOSFET static characteristics and switch-on Id transient are [4]: - If the body contact of thin gate oxide BC pMOSFET is left floating, the body potential depends mainly on the ECB direct tunneling current between the partial n+ poly gate and the n type silicon substrate. Therefore, this BC pMOSFET Vbody is drain voltage insensitive on a wide range of Vds and is strongly gate voltage dependent.

- This high body potential leads to a drive capability increase with low subthreshold slope and no kink effect if the body is not connected. A 25% Ion gain has been measured with no Ioff degradation.

- The transient behaviours result from the steady-state body potential mainly controlled by ECB tunneling current.



Fig. 1 Body contacted pMOSFET top layout and cross-sectional view from line A-A.



Fig. 2 Dominant direct tunnelling mechanism under strong inversion.



Fig. 3 Principle of a 1T-DRAM cell (a) write "1" is by ECB tunneling current which injects electrons in the body (b) write "0" is either by forward biasing the pn junction or by removing the electrons through a direct tunneling current.

This ECB tunneling current induces or sweeps out a large amount of electron charges into the body neutral region and consequently, provides the possibility to store the "1" or "0" binary states. The operation principle of this gate induced floating body DRAM is shown in the figure 3. During write "1" operation, the ECB component is used to inject electrons from the gate into the n body (Vg=-1 V). The body potential is more negative due to the majority carriers charge excess in the quasi-neutral zone. A threshold voltage shift is observed and a higher drain current is measured at Vg=-0.3 V (Fig. 4).

Power consumption of the write "1" operation is dramatically reduced by several orders of magnitude if ECB tunneling current is used instead of impact ionization or (GIDL). Contrary to these previous approaches, there is no drain current during write "1" operation because no voltage is applied to the drain. The power consumption is only due to ECB tunneling current which is 6 and 2 orders of magnitude lower than impact ionization and GIDL current [2]. If the source current is measured under continuous read conditions at both -100 mV and -500 mV drain voltages (Fig. 5 (a)), we observe a symmetrical degradation of state "0" and state "1". As a result, a sufficient memory window remains after 10 ms reading at room temperature. The recombination mechanisms which induce the body discharging and charging via the ECB tunneling current are the main mechanisms suspected to be responsible of the loss of data "1" and "0".



Fig. 4 Measured Id-Vg characteristics at Vds=-500 mV for states "0" and "1" (W/L= 5μ m/0.10 μ m).



Fig. 5 (a) After write "0" and "1", evolutions of the read current margin as a function of reading time measured at Vds=-100 mV and -500 mV (W/L=5 μ m/0.10 μ m). (b) Retention characteristics under reading conditions measured at Vds=-500 mV.



Fig. 6 Measured source current time dependencies at $Vds=-500mV (W/L=5\mu m/0.10\mu m)$.

Hold conditions have been optimized (Vg=-0.3 V) in order to reduce the electric field in the thin gate oxide and consequently to maximize the retention time (Fig. 5 (b)). Finally figure 6 shows the amplitude of the memory effect and the time dependence of source current for the "0" and "1" write/read operations. This amplitude is large enough to be sensed by a current mode sense amplifier.

3. Conclusion

The body potential of BC pMOSFET processed with thin gate oxide strongly depends on the direct tunneling current between partial n+ poly gate and n type silicon substrate. Thanks to this feature, a new concept of capacitor-less 1T-DRAM PD SOI pMOSFET has been experimentally demonstrated. This ECB tunneling current exhibits low power consumption during the write "1" operation.

References

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