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Electrical Characteristics of Engineered ZrO_2/SiO_2 Tunnel Barrier with a High-k HfO_2 Trapping Layer for Non-Volatile Memory

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1. Introduction

The SONOS-type memory device is very attractive candidates to realize the continuity of vertical scaling on flash memory [1]. However, the SONOS has fundamental problems in the trade-off between erase speed and data retention. Recently, Charge trap flash (CTF) memory devices based on tunnel barrier engineering (TBE) have received considerable attention due to many advantages such as fast programming, good retention, low power operation, high density integration and good reliability. Moreover, further improving of programming/erasing (P/E) characteristics can be achieved by using high-k materials [2], [3].

In this paper, the nonvolatile memory capacitor devices composed of engineered ZrO_2/SiO_2 (ZO) tunnel barrier and HfO_2 trapping layer were fabricated. The electrical characteristics were compared with a conventional single SiO_2 tunnel barrier.

2. Experimental

$TiN/Al_2O_3/HfO_2/ZrO_2/SiO_2/Si$ (MAHZOS) memory capacitor cell, which composed of 8 nm HfO_2 charge trapping layer and 20 nm Al_2O_3 blocking oxide layer was fabricated by using atomic layer deposition (ALD) system at 300 ˚C. After formation of thin ZO tunnel barrier, the forming gas annealing (FGA) process was carried out at 250 ˚C, 300 ˚C, and 450 ˚C in 2 % diluted H_2/N_2 ambient, respectively. Finally, control sample of single SiO_2 (5.1 nm) tunnel barrier (MAHOS) were fabricated with same process.

3. Results and discussions

Fig. 1 shows the TEM image of ZrO_2/SiO_2 layers on Si substrate. The thickness of deposited ZrO_2 and SiO_2 films were 2.9 nm and 2.1 nm, respectively. Fig. 2 shows the tunneling current characteristics of MZOS capacitors. The 300 ^oC annealed sample revealed a lower leakage current at 0.15 V and a higher tunneling current at 1 V than the initial state. Moreover, these characteristics were superior to single SiO_2 film with the same physical oxide thickness (POT). However, the current significantly increased again at 450 ^oC [inset fig.2]. Fig. 3 shows charge trapping characteristics of ZO tunnel barrier. The memory window (ΔV_{th}) decreased with increasing FGA temperature. Especially, there is no charge trapping effect (ΔV_{th} 0.004 V) at 450 ^oC. However, a leakage current significantly increased at this temperature. Meanwhile, a hump in CV curves due to the poor interface was observed from the initial state and FGA at 250 ^oC [inset fig.3]. From these results, the effective temperature of FGA process was 300 ^oC. Fig. 4 shows the P/E characteristics of the MAHZOS memory capacitor under ±8 V, ± 9 and ±10 V gate voltage. The MAHZOS memory capacitor has superior programming characteristics than that of the MAHOS memory capacitors. Especially, after programming at +10 V, 1 ms condition, the higher erasing speed was achieved by using the ZO tunnel barrier. These results are attributable to the enhanced tunneling sensitivity of engineered tunnel barrier. Fig. 5 shows the data retention characteristics of the MAHZOS and MAHOS memory capacitors. The charge loss was 48 % and 70 % for MAHZOS and MAHOS, respectively after 10 years. Fig. 6 shows the data endurance characteristics of the MAHZOS and MAHOS memory capacitor. The MAHOZOS has no significant window narrowing after 10^4 P/E cycles. While memory window of the MAHOS was reduced with P/E cycle from 1.03 V to 0.34 V. The reason for the better endurance characteristics of the MAHZOS after 10 years is an enhancement of erasing property from engineered tunnel barrier.

4. Conclusions

We fabricated the MAHZOS and MAHOS memory capacitors and demonstrated their electrical characteristics. The engineered ZO tunnel barrier has larger field sensitivity than that of single SiO_2 layer. It contributed to the higher programming and erasing speed of HfO_2 CTF memory devices. Also these features led to enhance the retention and endurance characteristics. Moreover, further improvement of tunneling sensitivity was obtained by using FGA process at 300 ˚C in H_2 (2%)/N_2 ambient. Therefore, the engineered tunnel barrier with ZO stacks were useful structure and the optimized heat process for the ZO tunnel barrier would be effective method for high-integrated non-volatile memory applications.

Acknowledgements

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References

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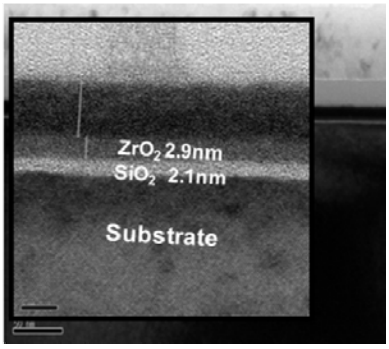

Fig. 1 TEM image of SiO_2/ZrO_2 layer on Si substrate.

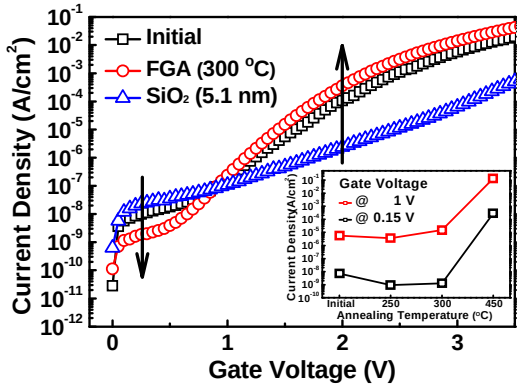

Fig. 2 J-V curve of MZOS capacitors at FGA 300 °C. Inset is tunneling current of MZOS capacitors versus FGA temperature.

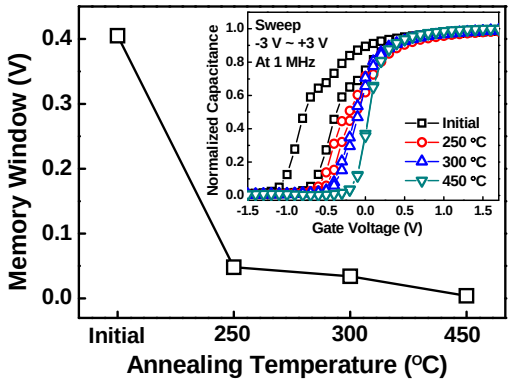

Fig. 3 Charge trapping characteristics of MZOS capacitors as a function of FGA temperature. Inset is hysteresis curves measured at 1 MHz and ±3 V sweep.

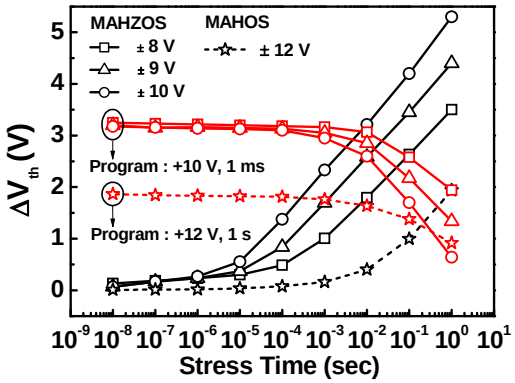

Fig. 4 Programming and erasing characteristics of MAHZOS and MAHOS devices.

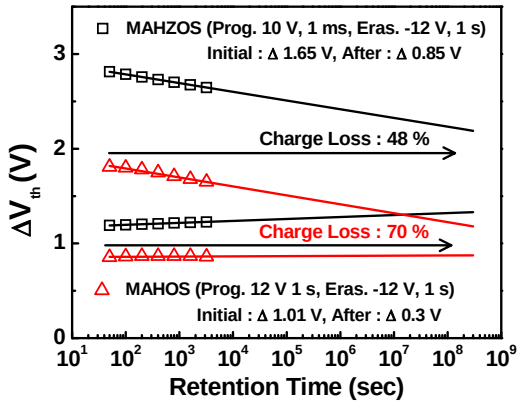

Fig. 5 Retention characteristics of MAHZOS and MAHOS devices at room temperature.

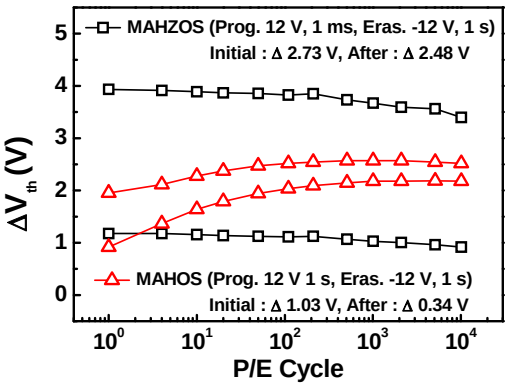

Fig. 6 P/E cycling endurance of the MAHZOS and MAHOS devices.