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Explanation of anomalous erase behaviour and the associated device instability in TANOS Flash using a new trap characterization technique

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Introduction and purpose:. Understanding and optimizing the erase behaviour of TANOS ($TaN/Al_2O_3/Si_3N_4/SiO_2/Si$) memory stacks is crucial for a reliable implementation of these devices. It has been observed in some cases [1,2] that, starting from the initial V_{fb} in a fresh device, an anomalous behaviour of the voltage/time transient occurs when a negative erase gate voltage is applied (Fig. 1). In this paper, we demonstrate that Al_2O_3 traps cause this anomaly. We demonstrate that an erase transient curve is a snapshot of the balance between positively charged hole traps in the nitride and compensating negatively charged Al_2O_3 bulk traps.

Experimental:. The processing of the stacks used in this study is summarized in Table 1. The stacks were selected for comparative study because of their distinct differences in erase behaviour (Fig.1).

Gate-Side TSCIS: in order to understand the erase transient, we first characterize the position and energy spectrum of electrical defects in the Al_2O_3 layer near the gate electrode. This can be achieved by **Gate-Side Trap Spectroscopy by Charge Injection and Sensing (GS-TSCIS)**, which is a significant extension of TSCIS, presented in [3]. Operation principle details are summarized in Fig. 2.

Although V_{fb}-shift is not a very sensitive measure for charge near the gate electrode, we still observe appreciable values vs. charge pulse time and amplitude (Fig. 3), indicating a large Al_2O_3 trap density resides near the metal electrode. Note that 4 nm bottom oxide prevents hole injection from the substrate into the nitride as long as the applied charge pulses are small in amplitude and time. Also, the trapping/detrapping of holes/electrons in the bottom layer is negligible for good quality SiO_2 and does not cause any V_{fb}-shift. The possible impact of nitride charge redistribution on V_{fb} is excluded by GS-TSCIS experiments on Al_2O_3/SiO_2 stacks. These samples show very similar V_{fb}-shifts under equivalent conditions (not shown). In conclusion, *all V_{fb}-shifts* in Fig. 3 *are due to electron trapping in the Al_2O_3 solely*.

The data of Fig. 3 are fed into an algorithm, similar as for TSCIS [3], that allows plotting the defect density vs. trap position and trap energy (Fig. 4). The three selected stacks show distinct differences. Stack 1 has a high trap density close to the gate but the steepest drop when scanning further away from the interface. In stack 2, the trap density drops more gradually, while in stack 3, a significant reduction in trap density is found, possibly due to the reduction of oxygen vacancies by reoxidation after Al_2O_3 deposition [4].

Link GS-TSCIS / erase transient: In Fig. 3, when $|V_{charge}|$ is large, we observe a turn-around in the V_{fb}/time curve, caused by hole injection from the substrate to the nitride. At this moment the GS-TSCIS becomes a 'slow erase' operation and the turn-around corresponds to the anomalous erase behaviour. At even higher $|V_{charge}|$, we find back the conventional erase transient characteristic of Fig. 1, but *with ~20 ms time resolution* on the determination of the V_{fb}-shift. Different from Fig. 1, this fast V_{fb}-measurement reveals an anomalous erase in *all* three stacks under study.

We can evaluate the anomalous erase behaviour in more detail through the experiment explained in Fig. 5. We apply V_G=-14V on stack 1 for in total 1s and dV_{fb} is monitored using ~20 ms interruptions at V_{sense} (region 1 in fig. 5). First, dV_{fb} increases slightly because of fast electron trapping in the Al_2O_3 traps, then a negative shift is seen because of substrate hole injection and trapping in the nitride.

After 1s at -14V, the gate voltage is switched (without interruption) to +2V (region 2 in Fig. 5). A fast V_{fb}-shift is observed, caused by the rapid discharging of electrons from the near-gate Al_2O_3 traps. In stack 1, V_{fb} saturates after ~1000s, indicating that the bulk Al_2O_3 trap density is low and the saturated V_{fb} reveals the true hole trapping in the nitride.

Stack 2 in Fig. 5 behaves similarly to stack 1, but the electron trapping is dominant, and even after 1000s at +2V, the net balance of trapped electrons in Al_2O_3 vs. trapped holes in the nitride still results in a positive V_{fb}-shift. Increasing V_G to +4V for 1000s or increasing the erase voltage is still insufficient to flip the balance in favour of nitride-trapped holes (Fig. 7). We also observe no saturation of V_{fb} in Fig. 5, concluding that the Al_2O_3 bulk trap density in stack 2 is so high that it will always dominate over the hole trapping in the nitride.

Finally, in stack 3 in Fig. 5, the near-gate Al_2O_3 trap density is significantly reduced, resulting in a small positive shift when applying V_G=-14V and, in region 2, the discharging is also limited. V_{fb} saturates after ~1000s, but shows limited hole trapping. This can only partially be attributed to the higher CET of the stack, since at increased erase voltage, the hole trapping remains limited. This indicates that a improvement of the Al_2O_3 can be compensated by a deterioration of the nitride hole trap density. Further optimization of both layers simultaneously remains needed.

The discharging of the bulk Al_2O_3-traps will determine the initial transient of retention characteristics, not only from erased state as shown here but also from programmed state, and needs to be included in the retention modelling.

Conclusions: When erasing a TANOS stack, a dynamic balance is created between trapped electrons in the Al_2O_3 and trapped holes in the nitride. Depending on Al_2O_3 trap density profile and measurement timing, this balance can be positive or negative. Al_2O_3 traps closer than ~2 nm from the gate interface are discharged in seconds when applying a small positive voltage (or even 0V), but traps further away from the metal gate discharge over a very long time period. This causes an inherent instability of the V_{fb} vs. time.

Acknowledgement: This work was performed under IMEC's memory program.

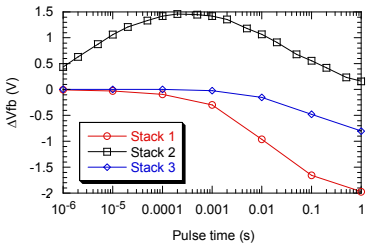
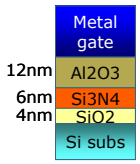


Fig. 1: TANOS erase transients at -16 V from fresh. Stack conditions are summarized in Table 1. These curves are obtained by applying short gate pulses followed by a V_{fb}-search routine, typically taking a few seconds to return the new V_{fb}. Stack 2 shows anomalous erase behaviour.



	post-Al2O3 treatment	Metal Gate
Stack 1	1000ºC N2	TaN
Stack 2	1000ºC N2	other Ta-based
Stack 3	reoxidation	TaN

Table 1: Summary of the stacks studied in this paper. Process splits are post-Al_2O_3 deposition

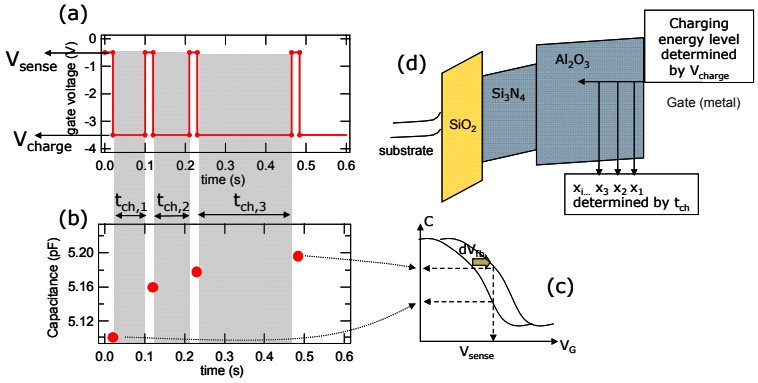


Fig. 2: The principle of Gate-Side TSCIS on capacitors with TANOS stack. By applying $V_{charge}< 0$ at the capacitor gate (Fig. (a)), the Al_2O_3 traps are charged by direct tunnelling from the metal gate as illustrated in the band diagram in Fig. (d). In order to measure the trapped charge density, the change of the capacitance is measured at V_{sense} , shown in Fig. (b). The interruptions at V_{sense} are short (~20ms), such that all charge sufficiently far away from the interface remains in the dielectric. The change of the capacitance is converted to a V_{fb}-shift using an initially measured CV-characteristic, illustrated in Fig. (c). The differences between TSCIS [3] and GS-TSCIS are: (1) trap densities near the top instead of the bottom electrode of the gate dielectric are scanned, (2) conventional TANOS samples with 4 nm bottom oxide are used, instead of dedicated samples with thinned-down (~1nm) bottom oxide. Furthermore, the use of capacitors instead of transistors broadens the applicability of the technique in [3] to structures that are easier and faster to process.

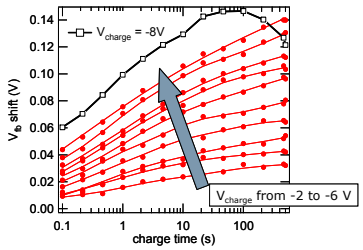


Fig. 3: Example of the V_{fb}-shift vs. charge time and voltage during GS-TSCIS. The top curve, taken at -8V shows a turn-around caused by substrate hole injection and subsequent trapping in the nitride. Therefore, only low |Vcharge|-values are considered in order to observe electron trapping in the Al_2O_3 only. Data are taken on stack 1.

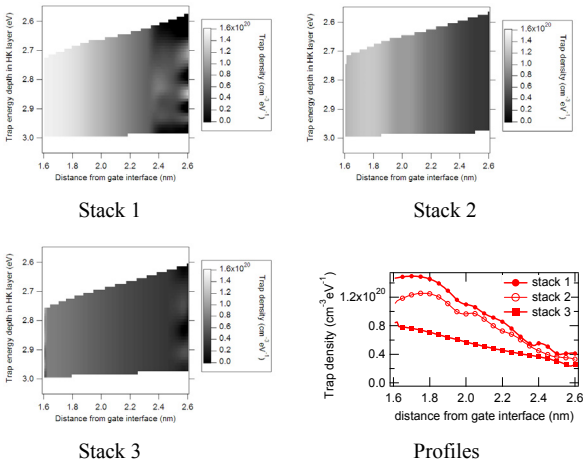


Fig. 4: GS-TSCIS trap density maps for stacks 1,2 and 3. The bottom right figure shows the spatial trap density profile of the average trap density between 2.8 and 2.9 eV below the Al_2O_3-conduction band edge.

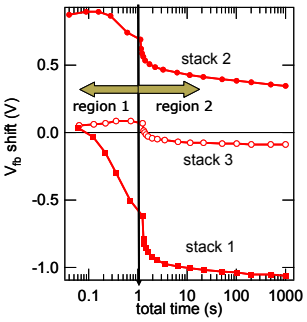


Fig. 5: The V_{fb}-shift vs time for stacks 1 to 3 when applying -14V during 1 s (region 1), immediately followed by +2V for 1000s (region 2).

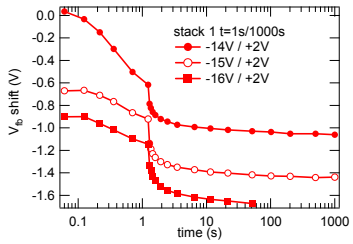


Fig. 6: Same measurement sequence as in Fig. 5, but repeated at increasing erase voltage on stack 1. All data are taken sub sequentially on the same device without interruption. Note that each time a new erase pulse is applied, the Al_2O_3-traps are again charged. Only after discharging the Al_2O_3 for long time, the true hole trapping is revealed.

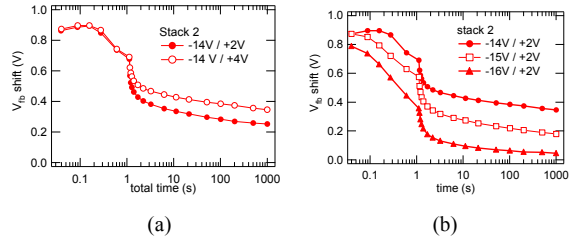


Fig. 7: Same measurement sequence as in Fig. 5 on stack 2. InFig. (a), the Al_2O_3-discharge voltage is increased, in Fig. (b) the erase voltage is increased. The net balance remains negative in all cases. The data in Fig. (b) are taken one after the other on the same device.

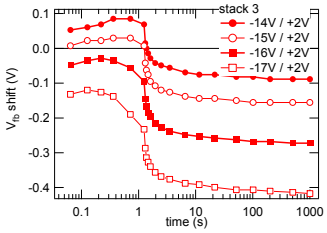


Fig. 8: Same measurement sequence as in Fig. 5 on stack 3. Even at an erase voltage of -17V, the hole trapping remains limited. All data are taken one after the other on the same device.

References:

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