Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp430-431

Precision Programming Power Control in Embedded P-channel SONOS Flash Using Transient-IV Method

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Abstract—The precise programming current estimation for SONOS-type flash memory employing a transient-IV method has been reported for the first time. With the real time current captured technique, the curves of the transient current vs. the threshold voltages are obtained to predict programming power precisely and reduce the pumping circuitry area in comparison with conventional method. Particularly for P-channel SONOS evaluations, it is helpful to achieve tighter on/off distributions under appropriate programming biases.

I. Introduction

Charge-trapping devices have attracted much attention in NVM embedded applications [1]. In the past, there were few attempts regarding the transient behavior of memory cells because it is hard to capture the real time current. In order to evaluate power consumption for pumping circuit design, conventional DC-IV method [2] is widely used to predict programming current in either N-channel or P-channel flash devices in Fig. 1. However, the accuracy was constrained due to stress during long-time measurement by applying voltages through SMU (**S**ource-**M**easure-**U**nit). It is overestimated when measuring the programming current of P-channel SONOS with **C**hannel-**H**ot-**E**lectron injection (CHE) mechanism because the conventional method would program the cells and lead to higher channel current of memory cell. To overcome this problem, a precise programming power control employing a transient current (transient-IV) method is demonstrated with embedded P-channel SONOS devices [3] ($0.18\mu m^2$ NeoFlash® shown in Fig.2 writing time < 100μs).

II. Experimental Setup

For a charge-trapping transient-IV evaluation, the first thing we concerned is how to extract transient current without additional mask or layout change on DUT (**D**evice-**U**nder-**T**est) while accurate and easy measurement can be kept. We outline equivalent circuits as shown in Fig. 3(a). It is a simple method but may lead a loading effect by connecting a resistor with source-line (SL) to probe the voltage drop which can be converted to programming current. In Fig. 3(b), resistor components are replaced by a current-to-voltage amplifier which not only can be virtual ground in input terminal but also be gain tunable plugged in the device. Figure 4 is the schematic of the transient-IV measurement setup. For CHE programming, the only pulse is applied on bit-line (BL), the DC voltages are applied on the word-line (WL) to invert the channel, and the control-line (CL) to create electrical field for electron injection. Then the transient current can be detected by oscilloscope via current-to-voltage amplifier.

III. Results and Applications

A p-channel transistor is tested by transient-IV method as shown in Fig 5, and we choose amplifier-B for NeoFlash® measurement because of nanoseconds level of raising and falling time. Figure 6 shows the characterizations of conventional DC-IV method for NeoFlash®, and it reveals the programming current is about 330μA at BL=-5.5V, WL=-4.5V. Figure 7 points that the WL transistor driving current is slightly smaller than the programming current predicted by DC-IV method. However, the transient-IV behavior as shown in Fig 8 describes the real time current is 225μA (at BL=-5.5V, WL=-4.5V) which is about 30% lower than prediction by conventional DC-IV method during 100μs programming time. The threshold voltages corresponding with time indicates that the programming speed is almost equal when WL < -3.5V as shown in Fig. 9. From above results, the curves of threshold voltages to the transient-IV can be plotted in Fig. 10. It can be used to estimate an accurate range about power consumption and a suitable WL bias for desirable threshold voltage window in memory cell. The similar result of BL = -6V is also shown in Fig. 11. Due to the high programming efficiency, the clamped channel currents make the power consumption decrease substantially but still maintain programming performance. Table 1 summarizes the comparison between conventional method and transient-IV method. It clearly points the DC-IV prediction for worst case of programming current is larger than transient-IV over 41% at criterion of $\Delta Vt > 3.5V$ and 100μs maximum program time. In other words, 41% pumping circuit areas could be saved since it is overestimated by conventional DC-IV method. Moreover, it is helpful to tighten PGM distribution in an array for byte program operation by applying optimized WL bias which makes channel current of WL transistor the same as programming current of memory cell. So the faster-bits are clamped by channel current of WL transistor and would not occupy the programming current of slower-bits as illustrated in Fig.12. It is no doubt narrower distributions for programming also enable narrower ones for erasing.

IV. Conclusion

In this paper, a simple transient-IV characterization method for charge trapping devices is proposed. We demonstrated and confirmed clearly the power consumption is overestimated compared with DC-IV method. The transient-IV method is helpful to evaluate pumping circuitry areas accurately and relieve unnecessary power dissipation. Furthermore, with the relationship between threshold voltages and transient current, optimized programming bias of WL could be found and hence cell distributions in P-channel SONOS devices would be tightened. The transient-IV method is also suitable for other advanced NVM devices such as RRAM.

Acknowledge

The authors would like to thank Hank Chiang who works for Keithley Instrument for technique support.

Reference

[1] C. Swift et al., IEDM Tech. Dig., p.927, 2002
[2] J.-H. Kim et al., VLSI Tech. Dig., p.31, 2003
[3] H.M. Lee et al., SSDM, p.196, 2005

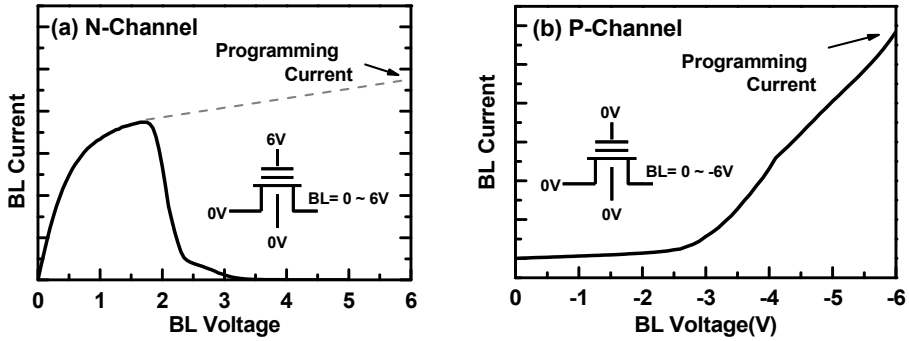

Fig. 1 Schematic of DC-IV method for program current prediction (a) N-channel (b) P-channel.

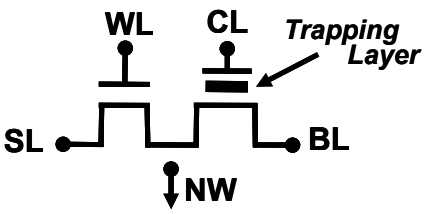

Fig. 2 Schematic of NeoFlash® cell structure.

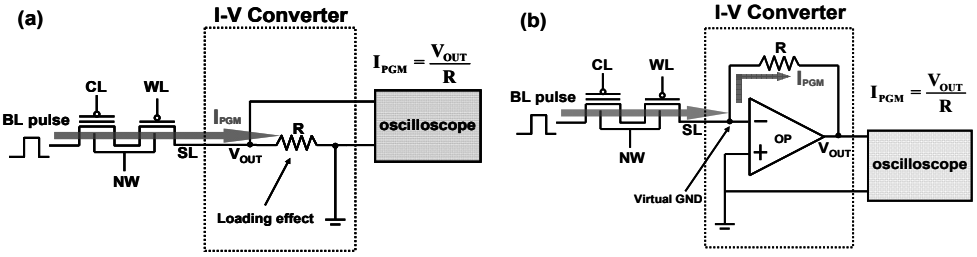

Fig. 3 Equivalent circuits for (a) with a resistor loaded and (b) with a current amplifier.

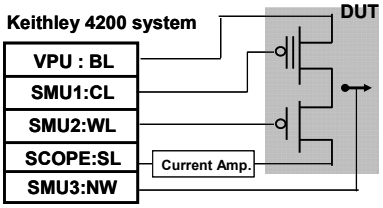

Fig. 4 Schematic of transient-IV setting.

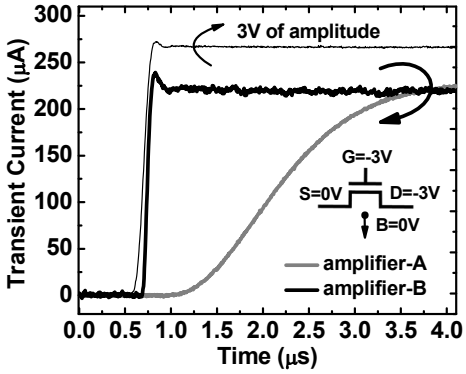

Fig. 5 Response time with different amplifiers.

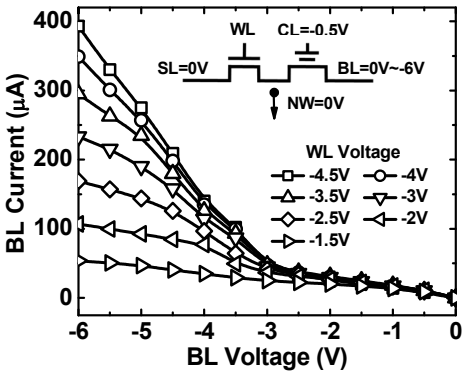

Fig. 6 DC-IV method for different WL biases.

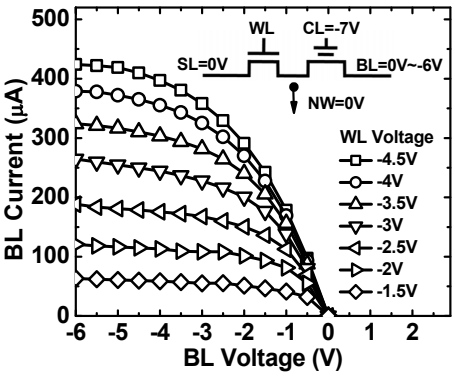

Fig. 7 The driving ability of WL transistor.

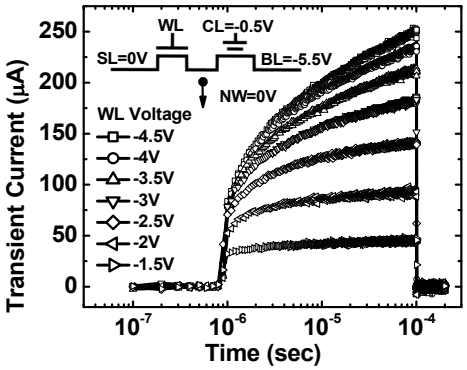

Fig. 8 Transient-IV for different WL biases at BL=-5.5V.

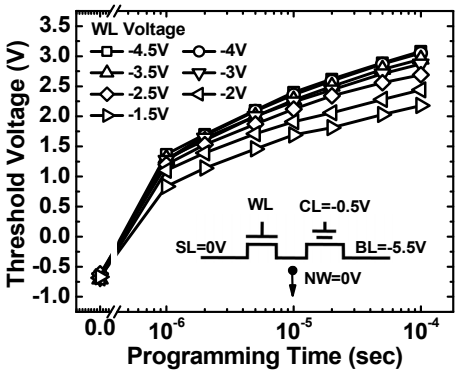

Fig. 9 Vt vs. time for different WL biases at BL=-5.5V.

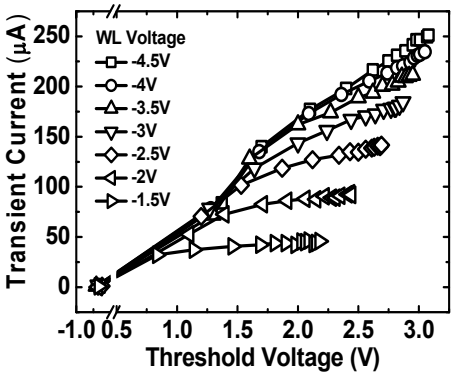

Fig. 10 Transient-IV vs. Vt plot at BL=-5.5V.

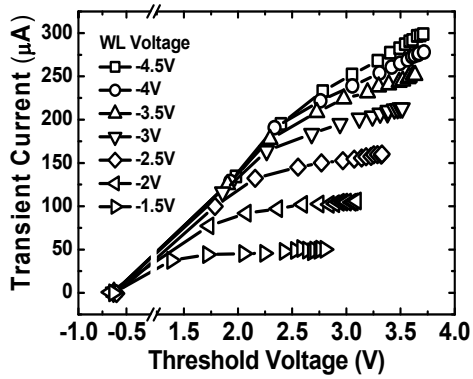

Fig. 11 Transient-IV vs. Vt plot at BL=-6.0V.

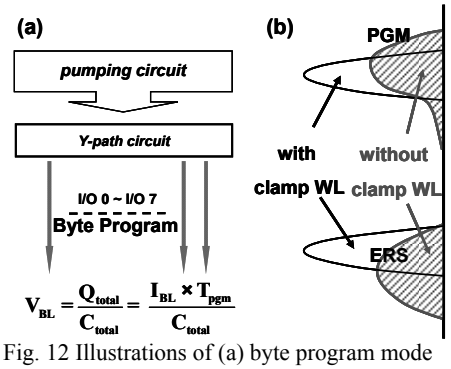

Fig. 12 Illustrations of (a) byte program mode in an array and (b) clamping WL bias to tighten PGM/ERS distribution.

Target @ ΔVT = 3.5V		WL=-3.5V	WL=-4.0V	WL=-4.5V
BL=-5.5V	Time	45μs	30μs	30μs
	DC-IV	260μA	300μA	330μA
	transient-IV	200μA	210μA	225μA
	offset	23.1%	30.0%	31.8%
BL=-6.0V	Time	5μs	5μs	5μs
	DC-IV	295μA	350μA	390μA
	transient-IV	210μA	220μA	230μA
	offset	28.8%	37.1%	41.0%

offset = (*DC-IV − transient-IV*) / DC-IV

Table 1 Programming current comparison between DC-IV & transient-IV methods.