Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp434-435

Source-Side Injection Programmed P-channel Self-Aligned-Nitride OTP Cell for 90nm Logic Nonvolatile Memory Applications

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1. Introduction

In the last several years, logic NVMs, nonvolatile memories made by standard logic process, have been in high demand in advanced VLSI circuits for code storage and customer settings. Conventional floating gate based memories suffers from the limitation of minimal gate oxide thickness as CMOS technology continues to scale [1-2]. A novel Self-Aligned-Nitride (SAN) OTP memory cell fabricated by standard CMOS logic process without any extra mask or process step has been proposed in our previous studies [3-5]. The programmed charges are stored in the self-aligned- nitride (SAN) spacers between the two closely placed gates. The SAN storage node is independent of the gate oxide, hence allows these cells to be realized in advance logic process beyond 90nm. In this paper, the successful development of an efficient and high speed programming scheme by source-side-injection hot electron (SSIE) injection is presented. This new programming method investigated for the p-channel SAN cell is found to enhance the overall performance of the SAN OTP cell for advanced logic applications.

2. Device Structure and Technology

The p-channel Self-Aligned Nitride (SAN) OTP devices investigated in this study are fabricated by the standard 90nm CMOS logic process. Fig. 1 and Fig. 2 show the cell layout and its cross-sectional TEM image, respectively. The SAN cell can straightforwardly be arranged in a NOR-type array, resulting in a very competitive unit cell size of 0.29 μm^2. The two gates are defined by the minimum feature size, while the spacing between the select gate (SG) and program gate (PG) is chosen to be 120 nm. The SAN storage node is consist of a layer of 150-180 Å lining oxide and a nitride layer of about 550-600 Å in thickness. For a p-channel device, to ensure the region under the storage node remains n-type, the p-type LDD implant is blocked by the modified the LDD mask.

3. Measurement Results and Discussions

Table I summarizes the operating conditions of the SAN cell in this study. The source-side-injection hot electron (SSIE) program operation is obtained by applying high voltage of both the program gate and source line, while slightly turn-on the select gate at -1V. Fig. 3(a) shows the simulated electric field along the channel during programming. We found that lateral electric field peaks near the PG edge and generates many highly energetic hole and electron pairs, as indicated in Fig. 3(b). The electron temperature distribution projected by simulation in Fig. 3(c) reveals that the high energy electrons mostly located right under the storage node, hence better program efficiency is expected.

As shown in Fig. 4, the programming characteristics under different bias conditions. The read current can change more than two orders of magnitude in less than 10 μs. In SSI operation, the select gate is biased right above threshold, so that the programming current is kept below 20μA, as shown in Fig. 5. Fig.5 also reveals that the drain current increases in the programming process. As more and more electrons are injected in to nitride region, the channel under the storage node turns on, and hence leads to an increase in programming current.

Fig. 6 compares the I_{BL}-V_{PG} characteristics of a cell in its fresh and programmed states. A read current window of more than 100X can be easily obtained. By adapting a different carrier injection mechanism from our previous work [3], data retention characteristics of the cell should be monitored. Fig. 7 shows that there is no significant charge loss after more than 1000hrs baked. The excellent charge storage ability is similar to NROM device as a result of the thick bottom oxide in the SAN node [6-7]. The program disturb characteristics shown in Fig.8 indicated that this cell can subject to over 1M disturb cycles from cells sharing the same WL.

Finally, Fig.9 shows that the cell can sustain continuous read above 10 years when bit line voltage is kept below -2.5V.

4. Conclusion

The logic compatible P-channel SAN cell realized by 90nm CMOS logic process can be programmed by highly efficient source-side injection scheme. With more than 100X read current window, high reliability, and disturb immunity, the Self-Aligned-Nitride cell has provided the promising solution for advance logic NVM applications.

References

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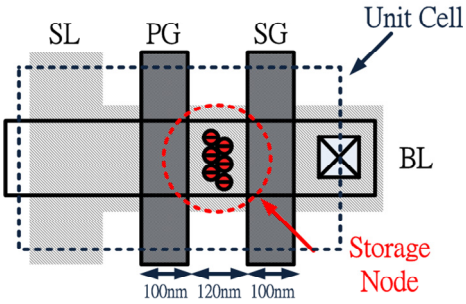

Fig. 1 90nm SAN cell layout with storage node defined by two gates.

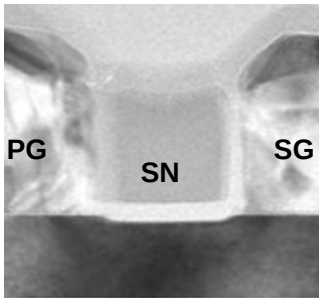

Fig. 2 TEM picture of the SAN storage node

Table I Operation Condition of the p-channel SAN OTP cell.

	PG		SG		BL		SL	
	select	unselect	select	unselect	select	unselect	select	unselect
Read	-1V	0V	-1V	0V	-1V	0V	0V	0V
Program	-9V	0V	-1V	0V	0V	float	-9V	0V

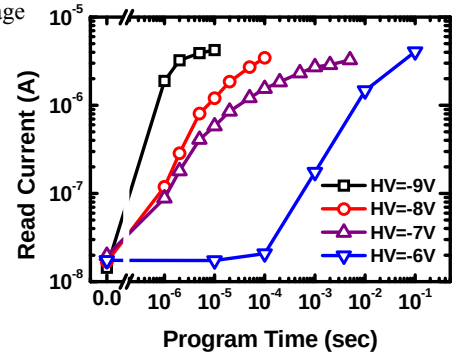

Fig. 4 Time to program characteristics of this p-channel SAN cell

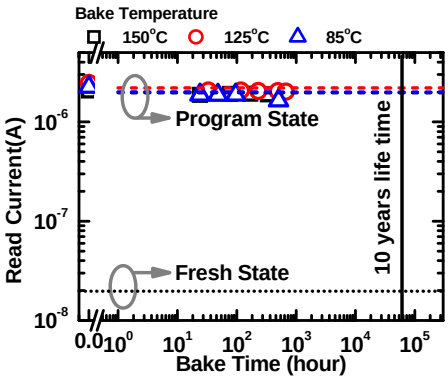

Fig. 7 Retention characteristics of the on-state current remain quiet stable under bake tests.

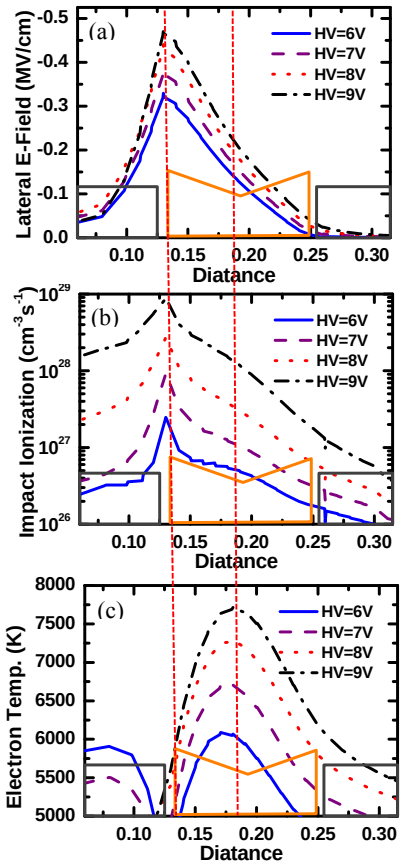

Fig. 3 The simulated (a) lateral electric field (b) impact Ionization rate, and (c) electron temperature along the channel.

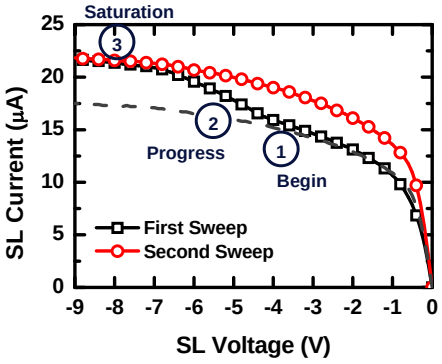

Fig. 5 Source-Side-Injection Hot Electron (SSIE) programming current shift.

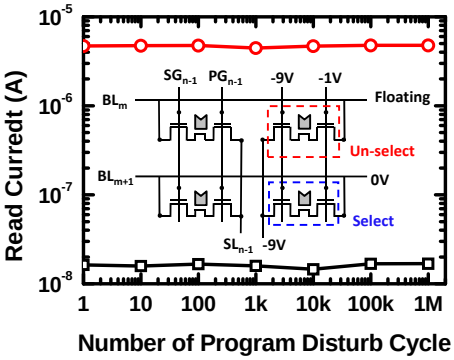

Fig. 8 Program disturb characteristics of the SAN OTP cell in a NOR array.

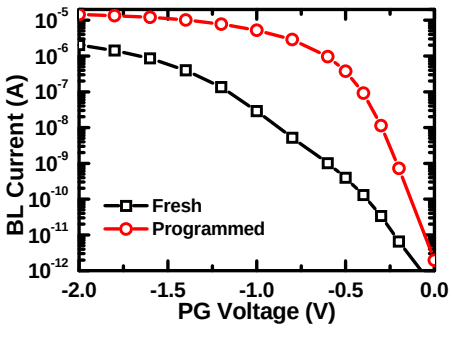

Fig. 6 The I_{BL}-V_{PG} characteristic shows large read current window under V_{PG}=V_{SL}=-1V.

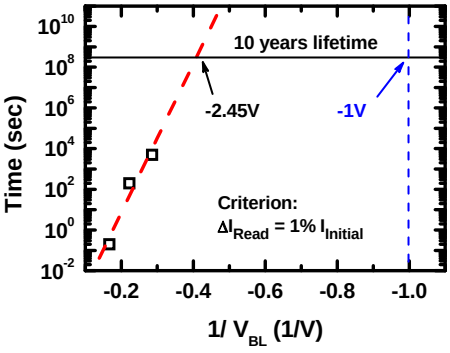

Fig. 9 The projected lifetime for read bitline voltage less than -2.45V is well above 10 years