Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp436-437

Optimized Silicon Nitride MONOS Memory for Superior Endurance of 10M Cycles

Kazuharu Yamabe, Shoji Yoshida, Yasuhiro Taniguchi, and Shiro Kamohara

Renesas Technology Corp., 751, Horiguchi, Hitachinaka-shi, Ibaraki-ken, 312-8504, Japan
Phone: +81-29-270-2428 E-mail: yamabe.kazuharu@renesas.com

Abstract

For excellent performance and reliability, Metal-Oxide-Nitride-Oxide-Semiconductor (MONOS) memory with optimized silicon nitride charge storage layer was investigated. By using optimized silicon nitride film instead of standard silicon nitride (Si_3N_4) film, fast Program/Erase (P/E) speed of 600μs, wide 3.0V Vth-window, good Vth-window of 1.1V after 10-year retention and wide 10M-cycled memory window of 3.0V are achieved.

1. Introduction

Smart card with contacts mainly is used as credit cards and mobile phone Subscriber-Identity-Module (SIM) cards. Recently, the contactless smart cards are gaining popularity for payment and ticketing applications such as mass transit.

For nearly 20 years, MONOS memory has been in production for these smart card applications. Compared to floating gate flash, MONOS memory is more scalable and highly reliable nonvolatile semiconductor memory.

Optimized silicon nitride film further extends the performance and reliability of MONOS memory without the difficulty and expensiveness of material engineering for high-k/metal gate stack.

Noted that the use of Ultra-thin Tunnel Oxide (UTO) is indispensable for superior cycling endurance without losing erase speed.

2. Experimental Procedure

The preparation of test device basically follows a standard NMOSFET process except that the gate oxide is replaced by an ONO structure.

First, the UTO (<2nm) was grown by thermal oxidation of silicon substrate. Then, the silicon nitride film was deposited by Low-Pressure-Chemical-Vapor-Deposition (LPCVD). Optimization of a silicon nitride film was controlled with ammonia (NH_3) to mono-silane (SiH_4) gas flow ratio [2]. For the blocking-top oxide, CVD oxide was deposited [3]. After the ONO stack was formed, poly-silicon was deposited and patterned.

To evaluate program/erase operation speed and data retention improvement, large cell size was used in this work. Program/erase were done by Vg control at Vs=Vd=Vsub=0V. The device is programmed by Modified Fowler-Nordheim (MFN) tunnel of electrons from the whole channel region [3]. On the other hand, the device uses Direct Tunneling (DT) of holes to erase. Since the device channel stays off during these operations, the power consumption is very low.

3. Results and Discussion

Fig.1 shows the Transmission Electron Micrograph (TEM) of the ONO stack with optimized silicon nitride. It was determined that the optimization of a silicon nitride film by Si/N ratio control was carried out without natural oxidation growth.

The program/erase characteristics of test devices are shown in Fig.2. Compared to standard silicon nitride device, optimized silicon nitride one exhibits fast program/erase speed of 600μs with wide 3.0V Vth-window. High-speed program/erase operation with low voltage less than 13V can be achieved due to the UTO.

Fig.3 compares retention characteristics of 500k P/E cycled test devices. Optimized silicon nitride device shows good Vth-window of 1.1V after 10-year retention at 85°C.

Fig.4 compares endurance characteristics of test devices at 85°C. Optimized silicon nitride device shows wide 10M-cycled memory window of 3.0V with fixed P/E time (600μs, 600μs).

Table I summarizes the memory data comparison. This work (SiO_2/Optimized SiN/SiO_2/poly Si) have done good memory device integrity of wide 3.0V Vth-window, good Vth-window after 10-year retention and wide 10M-cycled memory window of 3.0V. These results are the best data that have previously reported.

4. Conclusions

Optimized silicon nitride charge storage layer was investigated for MONOS memory application. Fast program/erase speed, wide memory window, better retention and superior cycling endurance are simultaneously obtained. It is concluded that this MONOS device is very promising for future flash memories.

Acknowledgements

The authors would like to thank T. Mine, N. Yabuoshi, D. Okada, K. Watanabe, K. Okuyama, H. Yoshida, K. Kuroda, M. Terasawa and K. Kubota for helpful discussions.

References

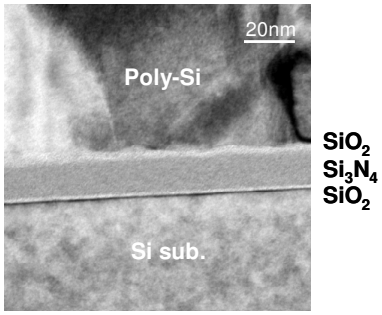
[1] S.-Y. Wang, H.-T. Lue, E.-K. Lai, L.-W. Yang, T. Yang, K.-C. Chen, J. Gong, K.-Y. Hsieh, R. Liu, and C. Y. Lu: *Proc. IRPS*, 2007, p. 171.

[2] T. Mine, K. Fujisaki, T. Ishida, Y. Shimamoto, R. Yamada, and K. Torii: *Jpn. J. Appl. Phys.* **46** (2007) 3206.

[3] S. Minami and Y. Kamigaki: *IEEE Trans. Electron Devices*, vol. 40, 1993, p. 2011.

[4] K.-H. Wu, H.-C. Chien, C.-C. Chan, T.-S. Chen, and C.-H. Kao: *IEEE Trans. Electron Devices*, vol. 52, 2005, p. 987.

[5] R. Ohba, Y. Mitani, N. Sugiyama, and S. Fujita: *IEDM Tech. Dig.*, 2007, p. 75.
[6] J.-S. Lee, C.-S. Kang, Y.-C. Shin, C.-H. Lee, K.-T. Park, J.-S. Sel, V. Kim, B.-I. Choe, J.-S. Sim, J. Choi, and K. Kim: *Jpn. J. Appl. Phys.* **45** (2006) 3213.
[7] C. H. Lai, A. Chin, H. L. Kao, K. M. Chen, M. Hong, J. Kwo, and C. C. Chi: *Symp. on VLSI Tech. Dig.*, 2006, p. 54.
[8] A. Chin, C. C. Laio, C. Chen, K. C. Chiang, D. S. Yu, W. J. Yoo, G. S. Samudra, T. Wang, I. J. Hsieh, S. P. McAlister, and C. C. Chi: *IEDM Tech. Dig.*, 2005, p. 165.
[9] C. H. Lai, A. Chin, K. C. Chiang, W. J. Yoo, C. F. Cheng, S. P. McAlister, C. C. Chi, and P. Wu: *Symp. on VLSI Tech. Dig.*, 2005, p. 210.
[10] I. Fujiwara, H. Aozasa, A. Nakamura, Y. Komatsu, and Y. Hayashi: *IEDM Tech Dig.*, 1998, p. 995.
[11] S. H. Lin, A. Chin, F. S. Yeh, and S. P. McAlister: *IEDM Tech Dig.*, 2008, p. 843.



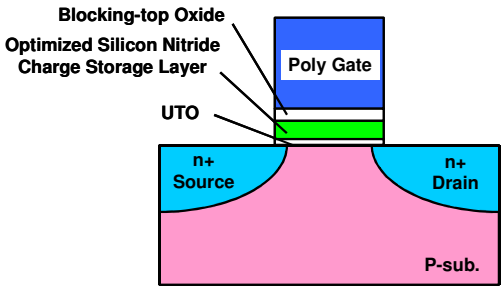


Fig.1 Transmission Electron Micrograph (TEM) of the ONO stack with optimized silicon nitride.

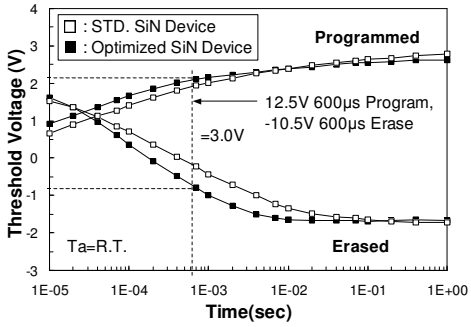


Fig.2 Program/erase characteristics of optimized silicon nitride device exhibits fast program/erase speed compared to standard silicon nitride one.

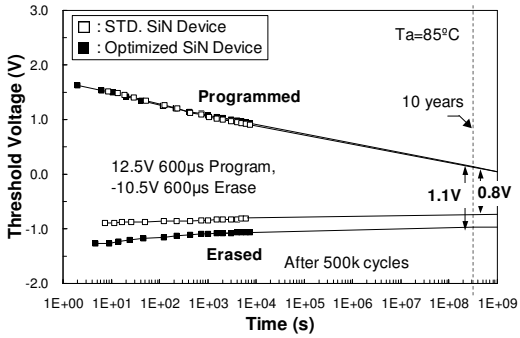


Fig.3 Retention characteristics of 500k P/E cycled optimized silicon nitride device have good Vth-window of 1.1V after 10-year retention at 85°C.

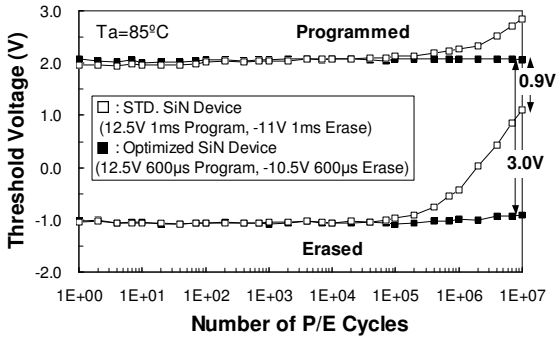


Fig.4 Endurance characteristics of optimized silicon nitride device have wide 10M-cycled memory window of 3.0V at 85°C.

Table I Comparisons of various MONOS Memory

	P/E condition for retention & cycling	*Initial Vth window*	*Vth-window after 10-year retention @85°C*	*Memory window @Cycles*
Smart Card Memory Specs	*<13V <600µs*	*>3.0V*	*>1.0V*	*>3.0V@>10M*
This work (SiO_2/Optimized SiN/SiO_2/poly Si)	12.5V 600µs/-10.5V 600µs	3.0	1.1	3.0@10M
BE-SONOS [1]	20V 500µs/-20V 10ms	>6.0	-	- @10k
Tapered band gap SiN SONOS [4]	12V 10ms/-10V 50ms	3.0	1.4	3.0V@1M
Double Junction Memory [5]	10V 200µs /-9V 200µs	1.8	0.9	1.8V@100k
TANOS [6]	17V 20µs/-19V 2ms	>6.0	-	0.2V loss@10k
SiO_2/HfON/HfAlO/TaN [7]	8V 100µs/-8V 100µs	2.5	1.45	2.1@100k
SiO_2/AlGaN/$AlLaO_3$/TaN [8]	11V 100µs/-11V 100µs	3.0	1.6	2.3@100k
SiO_2/AlN/AlHfO/IrO_2 [9]	13V 100µs/-13V 100µs	3.7	1.9	2.9@100k
Thicker tunnel oxide MONOS [10]	11.5V 0.7ms/-8V 80ms	1.8	1.0	1.8@1M
Charge-Trap-Engineered Memory [11]	16V 100µs/-16V 100µs	5.6	4.1	4.9@100k