Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp452-453

A Study of Packaging-induced Stress Distribution for Small-scale Silicon Chips

Naohiro Ueda, Eri Nishiyama and Hirobumi Watanabe

Ricoh Corporation, Electronic Devices Company
30-1, Saho, Kato, Hyogo 673-1447, Japan
Phone: +81-795-43-1123 Email: naohiro.ueda@nts.ricoh.co.jp

1. Introduction

With the rapid development of battery-powered devices recently, power management integrated circuits (ICs) need higher accurate operation to ensure safety with respect to the lithium-ion battery. Electrical parameters of each semiconductor parts such as transistors and resistors change from wafer condition due to piezo effect caused by mechanical stress generated by packaging process. This parametric change sometimes might cause fatal fluctuation of entire circuit performance. Despite the widely recognized importance of high precision, the impact of packaging induced performance change has rarely been examined, because small-scale analog chips, such as power management ICs, have a limited number of bonding pads, which makes the measurement of multiple points difficult.

The aim of this paper is to investigate residual stress distributions on the surface of a small-scale chip, which is smaller than 1.2 mm, experimentally for the purpose of further high precision of power management ICs. In addition, the impact of both silicon chip size and package structure was also clarified.

2. Experimental

In order to evaluate stress distribution for the small-scale chip with limited number of bonding pads, specially designed test chips and cantilever bending calibration system have been established [1]. A new technique that multiple data from different test chips with different piezoresistor locations are displayed simultaneously on a single chip area enables the distribution chart to be reproduced with only four pins (Fig.1). The displayed arrangement on a chip having 45 piezoresistor sensors in a 0.8 mm × 1.2 mm is shown in Fig.2. The size of a piezoresistor is approximately 0.03 mm in length so that lattice-like arrangement in the entire chip surface can be achieved. Each piezoresistance coefficient can be extracted experimentally through controlled application of a uniaxial loading by the calibration system (Fig.3), and thereby stress components can be finally calculated by algebraic manipulation.

3. Results and Discussion

Figs.4 and 5 show the distributions of the longitudinal (y-direction) stress; *Sy* and transverse (x-direction) stress; *Sx* components for 0.8 mm × 1.2 mm test chip, respectively. The maximum compressive stresses of both *Sy* and *Sx* were generated at the central area of the chip surface and then gradually decreased toward the chip edge. The maximum stress value is approximately 80 MPa for the longitudinal direction and 50 MPa for the transverse direction.

Next, stress distributions of three kinds of test chips were evaluated in order to clarify the relationship between chip size and residual stress. The dimensions of x-direction are the perfectly same in three samples, and those of y-direction were modified. The residual stress measured at the center of the chip surface is summarized in Fig.6. Both *Sy* and *Sx* are greatly influenced by the size of y-direction. *Sy* goes up when the size is increasing and *Sx* changes inversely with *Sy*. Besides, the stress component that is parallel to the chip long side is larger than the other. This result indicates that the test chip is in a state of bending deformation by volume shrinkage of the molding compound that has the largest thermal expansion coefficient among the materials of the sample. Because bending moment that introduces Sy is larger once y-direction size is bigger, and large y-direction size makes it difficult to bend the chip to generate *Sx* structurally.

The impact of package structure on residual stress was investigated. The two same test chips encapsulated with different types of packages were measured. Both of these chip size are 0.8 mm × 1.2 mm, outline drawings of two types of packages are shown in Fig. 7. The most remarkable feature of the two packages is that package B has smaller amounts of molding compound compared to package A. The comparison of *Sy* on chip central area is shown in Fig.8. The residual stress in package B is greatly decreased even though the chip size is perfectly same. Therefore small size of package is effective for reducing packaging induced performance change.

4. Conclusions

The residual stress that is generated by the resin-molded packaging process has been evaluated experimentally with specially designed test chips. The distribution of residual stresses greatly depends on the size of silicon chip, and bending deformation is the origin for introducing the stress. In addition, the impact of package structure on residual stress was clarified. As a result of this study, selection of package type should be paid attention to for further high accuracy of small-scale analog ICs as much as chip size.

References

[1] N. Ueda et al., "Evaluation of Packaging-induced Performance Change for Small-scale Analog IC," Trans. Semi. Manuf. vol. 22, No. 1, Feb. 2009.

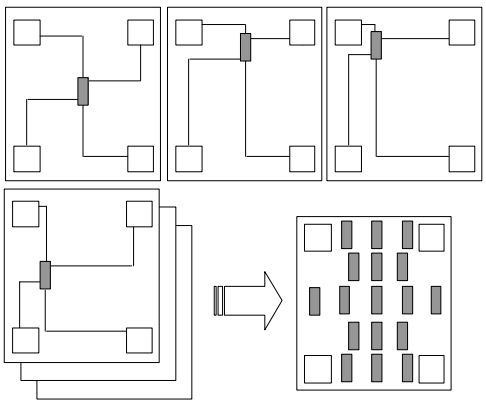

Fig. 1 Principle of multiple-point measurements using multiple test chips.

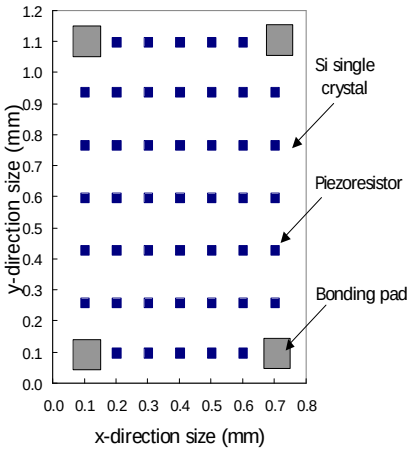

Fig. 2 lattice-like arrangement of 45 piezoresistors, chip size is 0.8 mm × 1.2 mm.

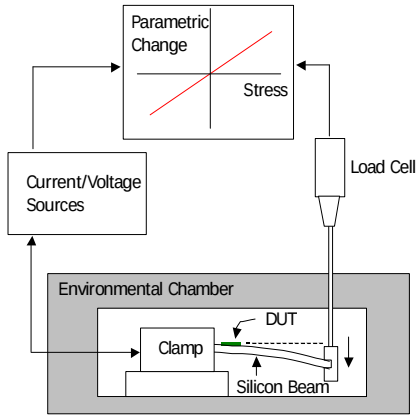

Fig. 3 Cantilever calibration system.

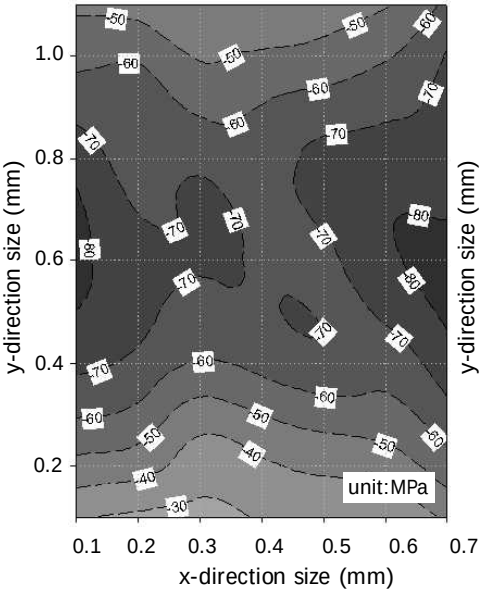

Fig. 4 Longitudinal stress distribution for a 0.8 mm × 1.2 mm Si chip.

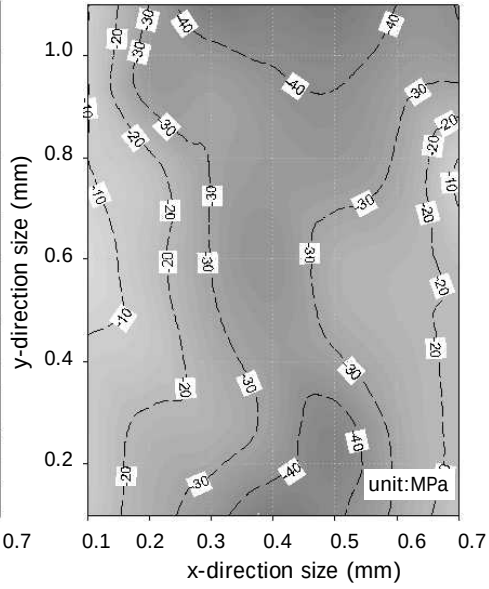

Fig. 5 Transverse stress distribution for a 0.8 mm × 1.2 mm Si chip.

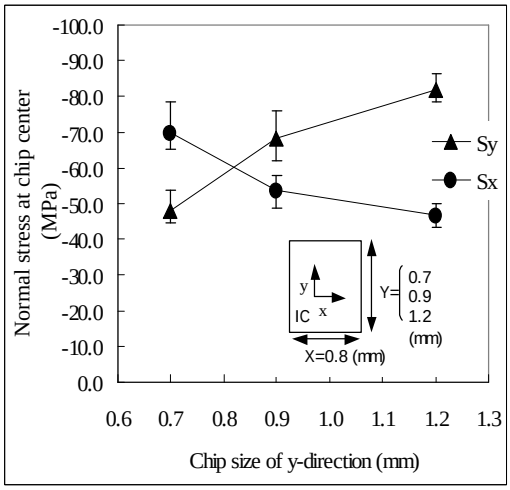

Fig. 6 Measurement results of residual stress components.

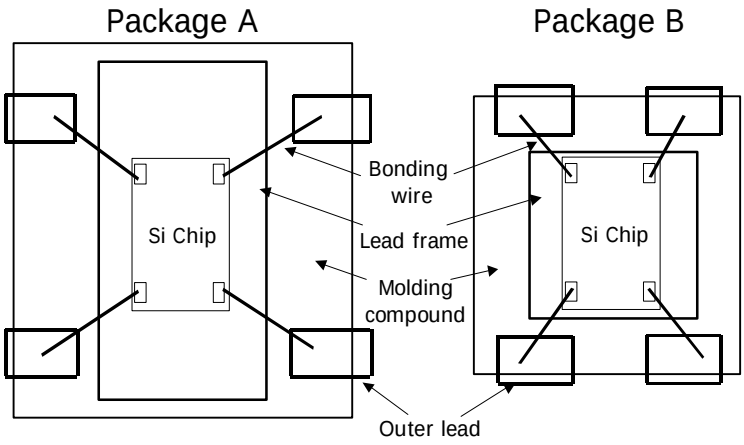

Fig. 7 Outline drawings of two types of packages.

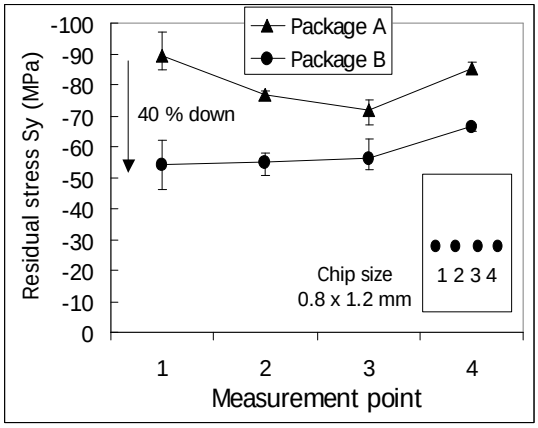

Fig. 8 Measurement results between two packages.