Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp456-457

31.25 ps Differential Equivalent Time Sampling Circuit Using 65 nm CMOS Technology

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1. Introduction

Impulse radio ultra-wide-band (IR-UWB) CMOS circuits have been developed for base-band transmission and radar applications [1] - [4].

In this paper, we propose a new equivalent time sampling circuit for the UWB cancer detection system. The system can detect an embedded dielectric target whose dielectric constant is different from that of the surrounding dielectric material. In this system, analog to digital converter (ADC) measures a time delay between the transmitted signal and the received signal which is reflected by the target. In order to detect a small target, the proposed circuit has 31.25 ps time resolution.

2. Detection System and Sampling Circuit

Detection System

The UWB radar system for embedded target detection is shown in Fig. 1. The system consists of transmitter (TX) and receiver (RX) circuits including a differential-input equivalent time sampling circuit with a differential ADC. Its sampling time is determined by a selected signal from the 16 phase output phase locked loop (PLL), synchronized with TX circuit. When the comparing at one sampling point is finished, the selected signal is changed to the next phase to sample the next point.

Equivalent Sampling Circuit

The proposed equivalent time sampling circuit with differential ADC is shown in Fig. 2 (a). 15 comparators compare the input voltage (V_{inp} - V_{inn}) with the difference of 2 reference voltages V_{rpx} and V_{rnx}. These voltages are divided into 15 levels of reference voltage (V_{rp} - V_{rn}) by the resistors. These comparators are operated by the sampling clock generated by the PLL and the selector. The sampling frequency is 125 MHz and the sampling interval is 31.25 ps. The 15 comparators generate a thermometer code.

After the comparison, the error corrector circuit corrects the error bit in the thermometer code by detecting the border between 0 and 1, then, the encoder converts 15 bit thermometer code to 4 bits digital code. In the majority circuit, the majority numbers of each bit are output.

Differential ADC

The proposed ADC is shown in Fig. 2 (b). This circuit consists of 1st and 2nd amplifiers and a cross-coupled circuit. The 2nd amplifier and the cross-coupled circuit are switched by a clock signal (CK). When CK is zero, the 2nd amplifier is active. Then, the amplifier compares the input signal (V_{inp} - V_{inn}) with the reference voltage. (V_{rpx} - V_{rnx}) When CK changes zero to VDD, the cross-coupled circuit become active and start to extend the output of the 2nd amplifier because of the positive feedback action. Even if the output of the 2nd amplifier is small, the cross-coupled circuit can amplify this output.

3. Measurement

Measurement Setup

The test chip, shown in Fig. 3, was fabricated by a 65 nm CMOS technology. The size is 1.85 mm x 0.9 mm. The measurement setups are shown in Fig. 4. When the sine wave is input, the inverted signal is generated by delay component. And, when the GMP signals are input, the signal is generated by synthesizing two narrow-width rectangular pulse signals. One of them is delayed and inverted. The measurement conditions are shown in table I.

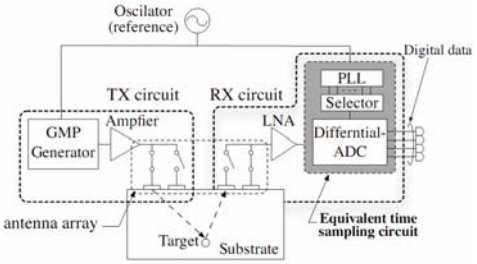
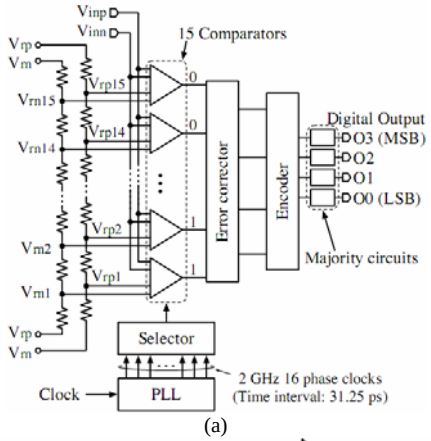
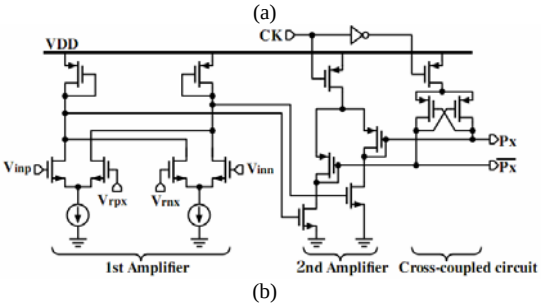


Fig. 1 The detection system



(a)



(b)

Fig. 2 Block diagram of equivalent time sampling circuit. (a) Proposed sampling circuit. (b) Comparator [5].

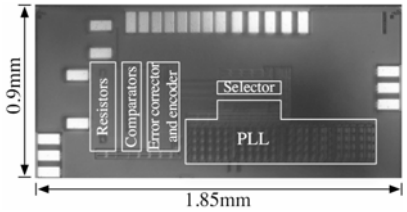
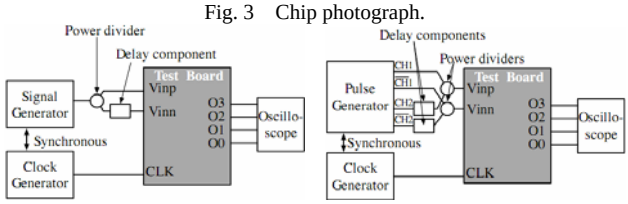


Fig. 3 Chip photograph.



(a) (b)

Fig. 4 Measurement setups. (a) Setup for sine wave input. (b) Setup for GMP input

Table I Measurement condition.

	sine wave	GMP
supply voltage	1.2 V	
refference voltage	Vrp: 0.82 V Vrp: 0.38 V	Vrp: 0.75 V Vrp: 0.45 V
amplitude	0.32 Vp-p	0.32 Vp-p
frequency	125 MHz - 750 MHz	450 MHz (center)
interval of pulse	-	8 ns

Measurement Result

First, the sine waves of a different frequency are input to the ADC from 125 MHz to 750 MHz. These results indicate the decrease of the output amplitude with increasing the input frequency as shown in Fig. 5. Each analog output is calculated from digital outputs. At the input frequency of 125 MHz, the amplitude is 12 LSB, which is nearly full level. However, when the input frequency increased up to 750 MHz, the output level decreased to 6 LSB.

Next, the GMP, shown in Fig. 6 (a), was input to the system. The magnitude is 320 mV_{p-p}, and its spectrum is shown in Fig. 6 (b). The envelope shows UWB signal and the center frequency is 450 MHz. Using this signal as an input, the sampling data are converted to digital signal. The measurement results of GMP are shown in Fig. 7. This result indicates the circuit can sample and convert the GMP signal.

4. Conclusions

We developed the differential-input equivalent time sampling circuit with 31.25 ps interval. Gaussian monocycle pulses having the center frequency of 450 MHz were sampled with time interval of 31.25 ps by the equivalent time sampling circuits using 65 nm CMOS technology.

Acknowledgements

This work is supported by the Semiconductor Technology Academic Research Center (STARC) and VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc and Mentor Graphics, Inc.

References

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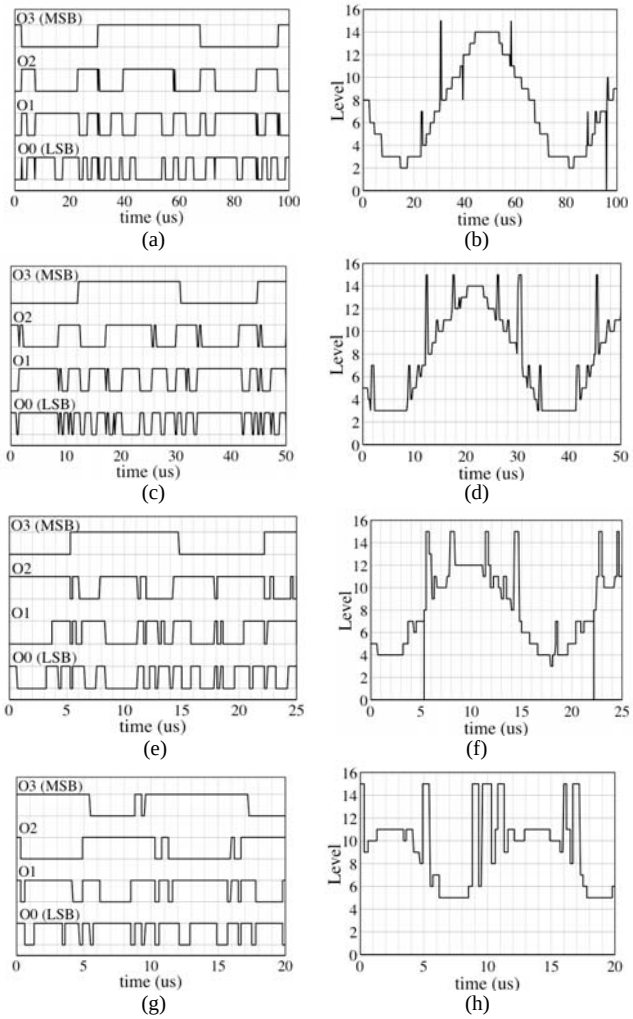

Fig. 5 Measurement results for 320 mV_{p-p} sine waveform. (a) Digital output (fin = 125 MHz). (b) Analog output (fin = 125 MHz). (c) Digital output (fin = 250 MHz). (d) Analog output (fin = 250 MHz). (e) Digital output (fin = 500 MHz). (f) Analog output (fin = 500 MHz). (g) Digital output (fin = 750 MHz). (h) Analog output (fin = 750 MHz)

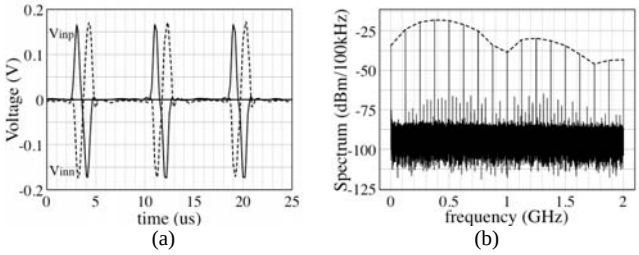

Fig. 6 Measured GMP signal. (a) Waveform. (b) Spectrum.

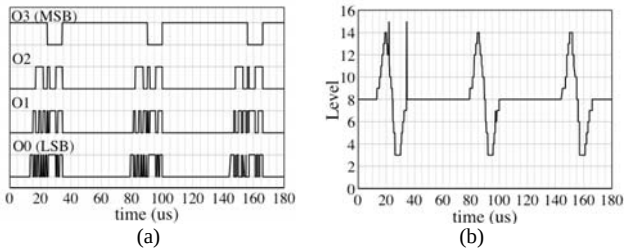

Fig. 7 Measurement results for GMP waveform. (a) Digital output. (b) Analog output.