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4 ch × 10 Gb/s Parallel Phase-synchronization Architecture and a Phase-adjuster Circuit using a Common Clock Signal

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1. Introduction

Due to the exponential increase in domestic and international Internet traffic, a new standard for optical and electrical communications is needed. The IEEE 802.3ba Task Force is therefore working to develop 40- and 100-G Ethernet as the next standard [1]. Because of the cost and technical limitations for speeding up of serial transmission, this task force is investigating the uses of parallel transmissions with wavelength division multiplexing (WDM) or ribbon fiber, such as 4 ch × 10 Gb/s, 4 ch × 25 Gb/s, and 10 ch × 10 Gb/s.

These parallel transmissions, especially long-distance WDM transmissions, need compensation for channel-to-channel skew caused by chromatic dispersion and temperature variation. One way to receive skewed signals is to phase-shift the sampling clocks. Another way is to phase-shift data[2]. Though both approaches need FIFO of the same depth to cancel all skew, the former needs a clock and data recovery (CDR) circuit for each data channel and uses each clock, while the latter makes the circuit simple with a common clock signal.

In this paper, we describe a phase-synchronization architecture that recovers a common clock signal from only one data signal and uses it for phase synchronization and signal reshaping. We also introduce a 4-ch phase-adjuster circuit for this architecture.

2. Phase–synchronization principle with variable-delay circuit

Our circuit architecture is shown in Fig. 1. It is composed of a clock multiplication unit (CMU), delay controllers, variable-delay circuits, and flip-flops. The CMU recovers a clock signal from the data signal of channel 1, In_1, because the data rate of each channel is identical in a parallel transmission. By means of phase comparisons of the common clock signal with the data signals of all channels, the delay controllers determine the amounts of delay and send control signals to the variable-delay circuits. The variable-delay circuits delay the data signals and minimize the phase differences of the data signals to the common clock signal. Finally, the flip-flops regenerate the data signals and synchronize them to the common clock signal.

The variable-delay circuit should have a variable-delay range of at least 1 UI for phase synchronization.

According to the SFP+ standard, the total jitter (TJ) for receiver is 0.7 UI at maximum. The eye-opening in the worst case is 0.3 UI. In such a case, the variable-delay circuit should have a delay resolution of less than 0.3 UI to recover the input data.

For the former target value, the phase-adjuster circuit utilizes variable-delay circuits, composed of eight-stage gate circuits, and flip-flops. For the latter target, it utilizes 8:1 selectors (Fig. 2). The variable-delay circuit delays the input data signal corresponding to the control signal provided from the delay controller.

3. Experimental results

A 4-ch phase-adjuster circuit was fabricated with

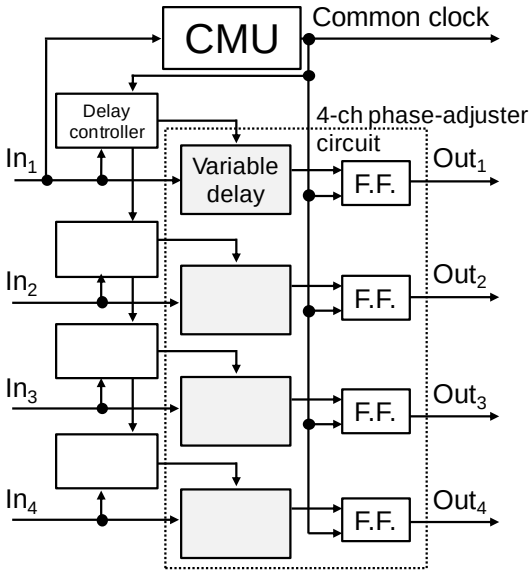


Fig. 1 Block diagram of the parallel phase-synchronization circuit.

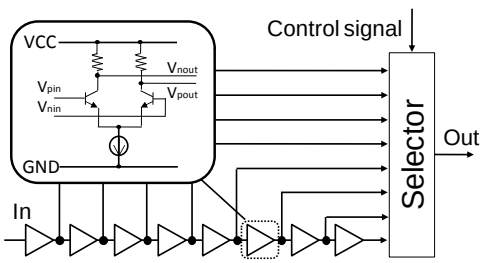


Fig. 2 Eight-stage variable-delay circuit.

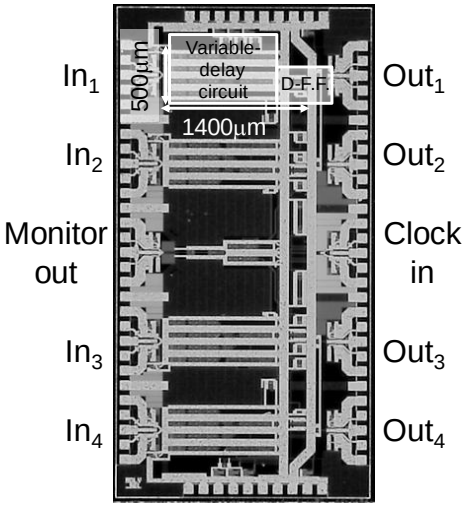


Fig. 3 Die photograph of designed phase-adjuster circuit

0.25-μm SiGe BiCMOS technology. Figure 3 shows a crograph of the test chip. The core of a phase-adjuster circuit occupies an area of 1.4 × 0.5 mm^2, and the whole 4-ch phase-adjuster circuit occupies 2.7 × 5.1 mm^2. The data rate was set to 10.3125 Gb/s, assuming 64B/66B coding, which is proposed in IEEE 802.3ba.

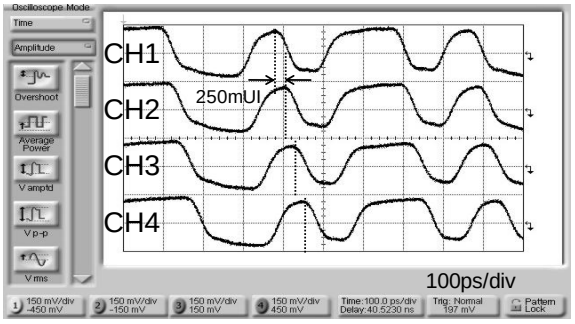
Figure 4(a) shows the input waveforms with skewed data patterns in 250 mUI steps and Fig. 4(b) shows the output waveforms aligned by the phase-adjuster circuit. The input data patterns were pseudo-random bit sequences (PRBS) of 2^7-1. We obtained a phase synchronization of all channels and error-free operation [bit-error ratio (BER) < 10^{-12}] when the numbers of delay stages for channel 1 to channel 4 were 1, 3, 5, and 7, respectively. Thus, the phase-adjuster circuit achieves phase synchronization and signal reshaping with a common clock signal. (Interchannel delays caused by wire-length differences in the chip are pre-compensated.)

Figure 5 shows the amount of cumulative delay amounts at respective stages for all channels measured by the monitoring circuit. The amount of delay at the first stage is located at the origin of the graph (Fig. 5). The total delay for the eight stages is over 120 ps and more than 1 UI at 10.3125 Gb/s (96.97 ps). These delays have small channel-to-channel variability and increase monotonically as the number of delay stage increases.

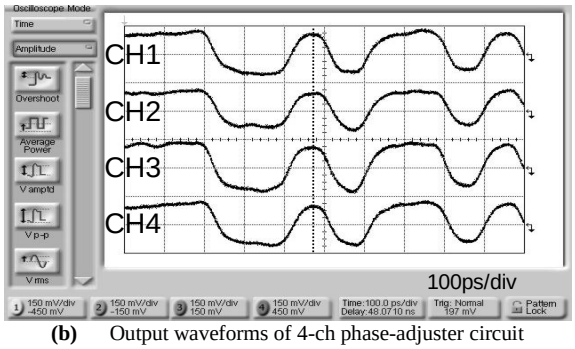
3. Conclusions

We described high-speed parallel phase-synchronization architecture. It uses only one CMU for phase synchronization and signal reshaping. For 4 ch × 10.3125 Gb/s, we fabricated and measured a 4-ch phase-adjuster circuit, which is composed of eight-stage variable-delay circuits and flip-flops. Measurement results show that the variable-delay circuit has the delay range of more than 1 UI, the delay resolution less than 0.3 UI, and it receives skewed data with a common clock.

This circuit achieves signal reshaping and phase synchronization without multiple CMUs. In comparison with other channel-to-channel deskew circuits [3][4], this architecture should reduce the chip size and power consumption.



(a) Skewed input waveforms



(b) Output waveforms of 4-ch phase-adjuster circuit

Fig. 4 Input and output waveforms with skewed data pattern.

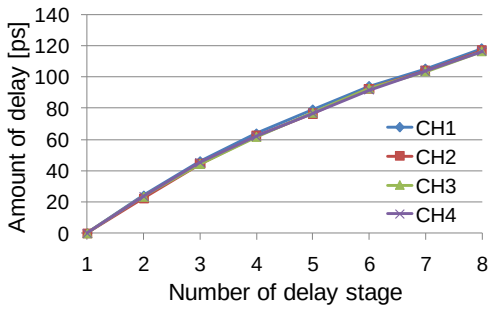


Fig. 5 Amount of delay at each delay stage.

References

[1]http://www.ieee802.org/3/ba/

[2]H. Kimura, Y. Sakai, and M. Tsubokawa, “An optical receiver module with over 9.6 nsec deskew range and 10 Gbit/s FMUX for a flexible optical access system based on PS-WDM-PON”, LEOS 2007, pp. 796–797

[3]M. Fukaishi, K. Nakamura, H. Heiuchi, Y. Hirota, Y. Nakazawa, H. Ikeno, H. Hayama, and M. Yotsuyanagi, “A 20 Gb/s CMOS multi-channel transmitter and receiver chip set for ultra-high resolution digital display”, ISSCC 2000, pp. 260 - 261, 463

[4]Y. Miki, T. Saito, H. Yamashita, F. Yuki, T. Baba, A. Koyama, M. Sonehara, ”A 50 mW/ch 2.5-Gb/s/ch data recovery circuit for the SFI-5 interface with digital eye-tracking”, ISSCC 2004, pp. 613 - 621