Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp460-461

An Optimal Design Method for CMOS Even-Stage Ring Oscillators Containing Plural Latches

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1. Introduction

Ring oscillators composed of a CMOS inverter chain are widely used due to their simple structure and low-voltage operation. In particular, the even-stage ring oscillators (ESROs), as shown in Fig. 1, are often used because 90° and/or 180° phase shift signals are easily obtained [1]. This circuit is composed of looped even delay inverters and a CMOS latch. In this circuit, the latch forces a couple of nodes (e.g. A and B in Fig. 1) in the loop to the opposite potentials to ensure continuous oscillation. To achieve a stable oscillation, we proposed the optimal design method for ESRO with a single latch using Static Noise Margin (SNM) analysis in Ref. [2]. The design method, however, requires that the triple SNM conditions are satisfied, and it is difficult to design the applicable circuit with this circuit topology.

2. Extension of the oscillation condition for ESROs with plural latches

In this paper, we extend the study to the case of ESROs with plural latches. When a second latch is added to the loop, there are essentially two cases as follows:

(a) the 2nd latch is placed at the even stage(s) after the 1st latch (e.g. Latch B for Latch A in Fig. 2).
(b) the 2nd latch is placed at the odd stage(s) after the 1st latch (e.g. Latch C for Latch A in Fig. 2).

In each case, the circuit diagram can be re-drawn using pseudo-SRAM topology shown in Fig. 3 (a) and (b).

In the case shown in Fig. 3(a), as stated in Ref. [2], SRAM1 must satisfy the triple SNM conditions as shown in Fig. 4(a):

(i) RSNM_L(Read SNM Low)>0 that means A3 ≠ B3 when (A1, B1)=(L, L).
(ii) RSNM_H(Read SNM High)>0 that means A3 ≠ A1 when (A1, B1)=(H, H)
(iii) WSNM(Write SNM)>0 that means node voltage (A3,B3)=(A1,B1) when A1 ≠ B1.

In Fig. 3(a), the output signals of SRAM1 (A3,B3) are applied to the input nodes of SRAM2, therefore SRAM2 must also have the same triple margins to oscillate the circuits. Therefore, this case still requires the same design restriction as for a single latch case as shown in Fig. 1.

On the other hand, in Fig. 3(b), odd numbers of inverters are inserted between the output of SRAM1 and the input of SRAM2. This means the input signals of SRAM2 are the inverted signals of SRAM1 outputs. In this situation, if both SRAM1 and SRAM2 lack RSNM_H as shown in Fig. 4(b), and if (A1, B1)=(H, H), then the outputs of SRAM1 (A3, B3) degenerate to (H, H). In this case, the state A3 ≠ B3 for stable oscillation cannot be achieved. However, the input signals of SRAM2 (A4, B4) are (L, L) because they are the inverted signals of A3 and B3. Therefore, if RSNM_L of SRAM2 is kept positive, SRAM2 achieves A6 ≠ B6 at its output, and ultimately the circuit can continue to oscillate. Hence, in the Fig. 3(b) topology, the oscillation condition does not require both RSNM_H>0 and RSNM_L>0, and thus it is drastically relaxed.

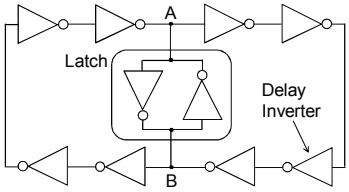


Fig. 1. An even-stage ring oscillator (ESRO) circuit.

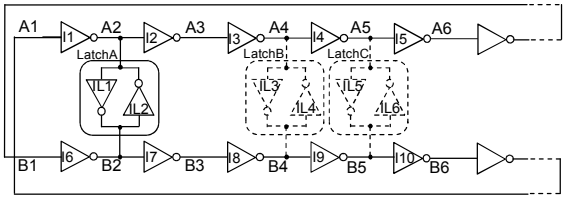
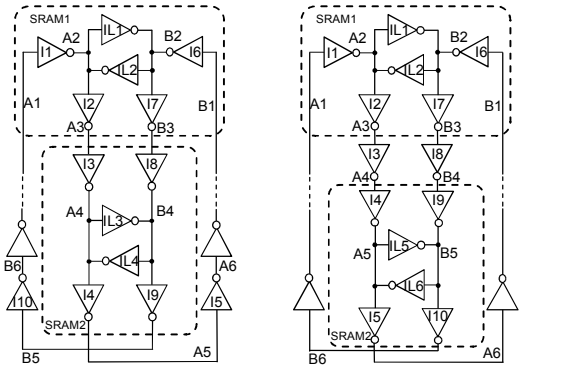
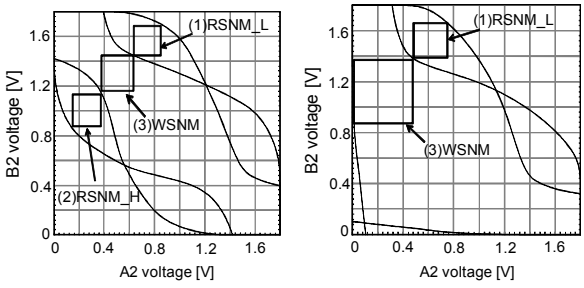


Fig. 2. An ESRO with multiple latches.



(a) A latch added at the even stage (b) A latch added at the odd stage

Fig. 3. Pseudo-SRAM circuit diagrams for ESROs with 2nd latch.



(a) Triple margin satisfaction (b) Lack of RSNM_H

Fig. 4. SNM characteristics.

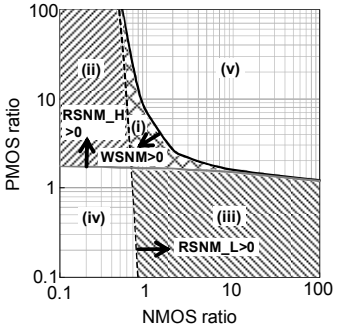
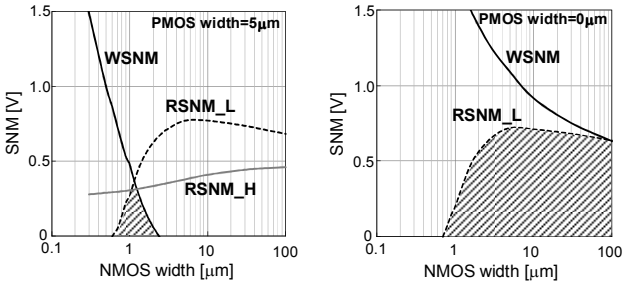


Fig. 5. Allowable design regions for ESRO circuits.



(a) with latches in EVEN position. (b) with latches in ODD position.

Fig. 6. Design margins for even-stage oscillators.

3. Design margins for ESROs

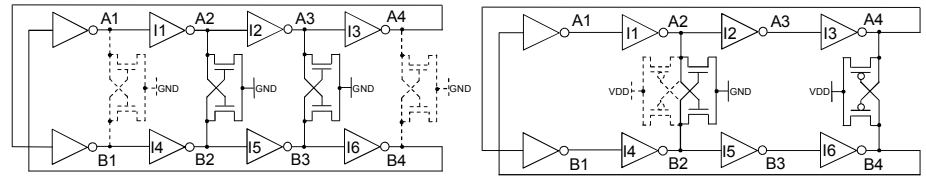
In this section, the design margins for ESROs will be discussed. Fig. 5 shows the regions in which three SNM values are larger than zero corresponding to the PMOS and NMOS sizes in the latch inverters. A standard 0.18-μm CMOS process technology and PMOS/NMOS gate width ratio for a delay inverter of 2 was assumed in this simulation. The vertical/horizontal axes show the PMOS/NMOS gate width ratio of the latch inverter to the delay inverter.

For the oscillator with a single latch, all three SNMs must be positive, thus only region (i) can be available. However, by adding another latch at the position of the odd stage, the oscillation condition is relaxed to that of either WSNM and RSNM_L or WSNM and RSNM_H being positive. This means region (ii) or region (iii) is added to the allowable region for circuit design.

The result of Fig. 5 also indicates that the single-channel latch, in which PMOS ratio=0 or NMOS ratio=0, can be utilized. It always ensures the WSNM is positive and also can contribute to achieving the small occupied area. Fig. 6 shows SNM values for Fig. 3(a) and (b) circuits corresponding to the NMOS gate width (Wn). In Fig. 6(a), the region in which all three SNM values are positive is Wn = 0.6 ~ 2.4 μm (the hatched area). On the other hand, in Fig. 6(b), the required condition is Wn ≥ 0.7 μm, therefore the design margin for stable oscillation is significantly widened due to inserting another latch in the correct position. Fig. 7(a) shows an example circuit. Two latch circuits in Fig. 7(a) are composed of only NMOS transistors, and both RSNM_L and WSNM are kept positive. To obtain symmetrical multi-phase waveform outputs, a latch can be inserted in every stage as shown in dotted lines.

4. Study on the relationship between the insertion position and polarity of latches

Fig. 7(b) shows another circuit example, where the 2nd latch circuit in Fig. 7(a) is shifted to the next stage, and its polarity is changed from NMOS to PMOS for which RSNM_H and WSNM are both positive. In this circuit topology, because the input signals of the pseudo-SRAM circuit are inverted by shifting the latch to the next stage, the complementary latches placed at the even stages with respect to each other guarantee oscillation. The circuit topology in Fig. 1 is regarded as the special case, in which complementary single channel latches are placed at the same stage as shown in dotted lines in Fig. 7(b). Fig. 8 shows the simulated waveforms for the nodes A1, A3, B1, B3 of the circuit shown in Fig. 7(b). It can be seen that approximately 90° phase shifts are achieved by adjusting the latch transistor sizes appropriately instead of inserting a latch to each stage.



(a) Oscillator with NMOS latches (b) Oscillator with NMOS/PMOS latches

Fig. 7. Oscillator circuits with single-channel latches.

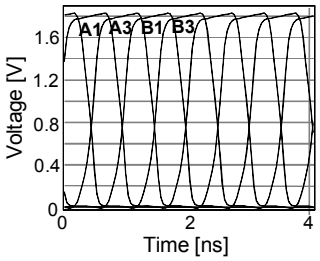


Fig. 8. 90° phase shift oscillation waveforms.

5. Conclusions

The design method for ESROs with plural latches was analyzed in detail. We clarified that the range of stable oscillation conditions can be drastically widened by the appropriate design of the polarity for the latch circuit and their insertion position. In this case, the single-channel latch is better than a CMOS latch. When the polarities for the two latches are the same, the latches should be placed at the odd stages with respect to each other. On the other hand, when the polarities are complementary, the latches should be placed at the even stage with respect to each other.

Acknowledgments

The VLSI Design and Education Center (VDEC) of the University of Tokyo, in collaboration with the Rohm Corporation and the Toppan Printing Corporation, provided the physical design parameters for VLSI design. This research was partially supported by funds from the Japanese Ministry: MEXT via the Kyushu knowledge-based cluster project.

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[2] K. Nakamura et al, *Extended Abstract of 2008 SSDM*, pp. 480-481, Sep. 2008.