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Design of an 8-nsec-search 72-bit-word Content-Addressable Memory Using Phase-Change Devices

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1. Introduction

Storage density and reliability of content-addressable memories (CAMs) have been continuously improved from the viewpoints of both device technologies and architecture [1]–[5]. Although CAMs for network routers require higher levels of reliability, errors in their stored data cannot be corrected during search operations. It is thus essential to improve the reliability of storage devices.

Phase-change devices not only have good scalability and resistance ratios higher than ten but also have good robustness against ionizing radiation [6]. These advantages make phase-change devices potentially suitable for a highly reliable CAM. Accordingly, in this study, we designed a CAM using phase-change devices and clarified its architecture, performance, and required resistances.

2. Architecture

The proposed resistive CAM cell incorporates two storage devices, SD0 and SD1 (i.e., phase-change devices) in an XNOR circuit (Fig. 1). Although this simple structure suppresses the area of a memory cell, it requires a careful circuit design to discriminate match-line current, which includes leakage current in one half of the memory cell (that is, a memory element) whose search line is activated (Table 1).

In the case of a conventional plane match-line structure, the ratio of match-line currents under the unmatched condition to those under the matched condition, α_P, is expressed as follows:

$$\{I_{ON} + (n-1)\times I_L\}/(n\times I_L) \le \alpha_P \le I_{ON}/I_L. \quad (1)$$

Here, n, I_{ON}, and I_L are the number of memory cells located on the match line, the turn-on current under the unmatched condition, and the leakage current under the matched condition, respectively. Since 72 memory cells are located on the match line in a standard CAM, leakage currents cannot be neglected. For example, when a match-line sensing circuit requires $\alpha_P \ge 10$, I_{ON} must be more than 1,000 times larger than I_L. This means that the phase-change resistance under amorphous state, R_0, must be more than 1,000 times higher than the resistance under crystalline state, R_1. This restriction complicates the design of a device.

To reduce resistance ratio β_R ($=R_0/R_1$), a one-hot-spot block code (OB code) (Fig. 2) and a hierarchical match-line structure (Fig. 5(a)) [2] are implemented in the proposed resistive CAM. In the case of per-two-bit coding, the ratio of match-line currents, α_H, is given by

$$\alpha_H \ge I_{ON}/(3\times I_L) \quad (2)$$

Thus, β_R is reduced by one order of magnitude.

3. Performance of search operation

Retention time and operating condition

The retention time of the resistive CAM during search operations, t, depends on the search cycle time and the search power consumed in the memory element, P. Although a higher pre-charge voltage, V_{PC}, is desirable to perform a single-end sensing (Fig. 5(a)), it enhances destruction of stored data. Since look-up tables in network routers are, however, updated periodically, one-day retention is sufficient for CAMs targeting this usage. In this case, the operating condition, namely, 8-ns cycle time (including 1.5-ns search-line activation) and 0.85-V pre-charge, is derived from Equation (3) [7] (Fig. 3).

$$t = D\exp\left[E\Big/\left\{kT_a + \frac{P}{P_1}\left(\frac{E}{\ln\left(t_1/D\right)} - kT_a\right)\right\}\right] \quad (3)$$

Memory element

The area of the memory element, based on 130-nm CMOS technology, was evaluated. In this evaluation, the effective area, including the sensing transistor of the match line and a pre-charge switch, was 200 F^2 (F: minimum feature size), as listed in Table 2. Moreover, typical models of phase-change resistances for circuit simulations have the same non-linearity as those of Ref. [8] (Fig. 4).

Performance evaluation and required resistances

In a circuit simulation under eight operating conditions, 8-ns cycle search operations were performed successfully (Figs. 5 and 6). As shown in Figure 5(b), 0.9-ns search-line activation is short enough for one-day retention. As shown in Figure 6, for the match line at 0.85 V, R_0 must be higher than 12 MΩ and R_1 must be lower than 97 kΩ. The minimum of the resistance ratio, β_R, is 123 and the minimum ratio of match-line currents, α_H, is 40.

4. Summary

A resistive content-addressable memory (CAM) using phase-change devices was designed. To reduce resistance ratio, β_R ($=R_0/R_1$), of the CAM, a hierarchical match-line structure and an OB code were implemented. As for the phase-change devices, for 8-ns search operation, the following characteristics are required: one-day search retention, R_0 of more than 12 MΩ and R_1 of less than 97 kΩ (i.e., β_R =123).

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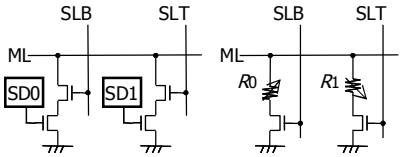


(a) Conventional (b) Proposed

Fig. 1: Concept of memory cell

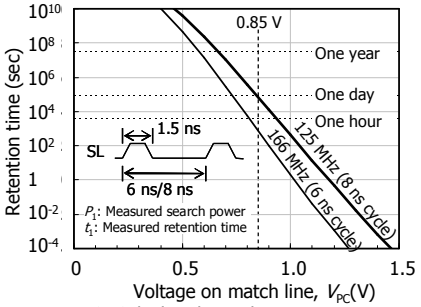


Fig. 3: Calculated search-retention time

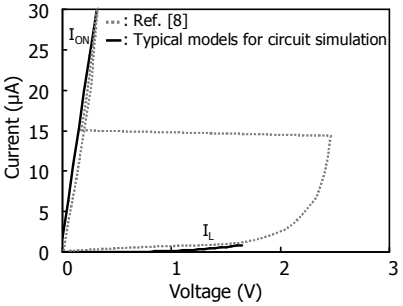


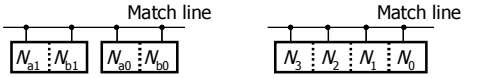
Fig. 4: I-V characteristics of phase-change devices

Table 1: Comparison of match-line currents during search operation

	Plane match line with *n* cells	Hierarchical match line featuring OB code
Matched	(Search key '1') SLB: L, SLT: H; (Stored data '0')	SL: H
current	$n \times I_L$	$I_{ON} \sim 4 \times I_{ON}$
Unmatched	(Search key = '1') SLB: L, SLT: H; (Stored data '1')	SL: H, SL: L
current	$I_{ON} + (n-1) \times I_L \sim n \times I_{ON}$	$0 \sim 3 \times I_L$

Data combination	Conventional ternary code: Notation (a_1, a_0)	Conventional ternary code: Stored-data pattern (N_{a1}, N_{b1}_N_{a0}, N_{b0})	One-hot-spot block code: Stored-data pattern (N_3, N_2, N_1, N_0)
0	00	01_01	0001
1	01	01_10	0010
2	10	10_01	0100
3	11	10_10	1000
0, 1	0X	01_00	0011
2, 3	1X	10_00	1100
0, 2	X0	00_01	0101
1, 3	X1	00_10	1010
1, 2	-	-	0110
0, 3	-	-	1001
0-2	-	-	0111
1-3	-	-	1110
0, 2, 3	-	-	1101
0, 1, 3	-	-	1011
0-3	XX	00_00	1111
None	-	-	0000

(a) Code mapping

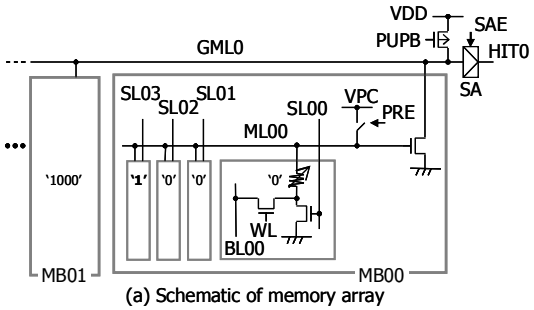


(b) Conventional word structure (C) Hierarchical word structure

Fig. 2: Concept of one-hot-spot block code (OB code)

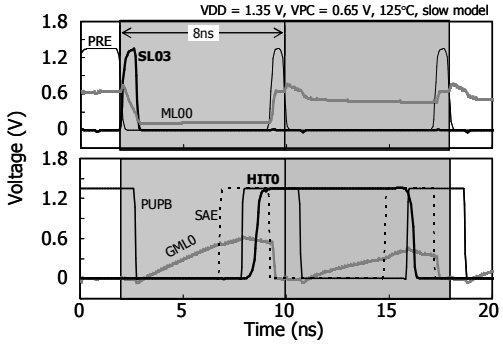
Table 2: Comparison of memory-cell areas

SRAM-based [9]	DRAM-based [9]	PCM-based (effective)
7.63 μm²	3.59 μm²	3.29 μm² (6.77 μm²)
451 F^2	212 F^2	194 F^2 (400 F^2)



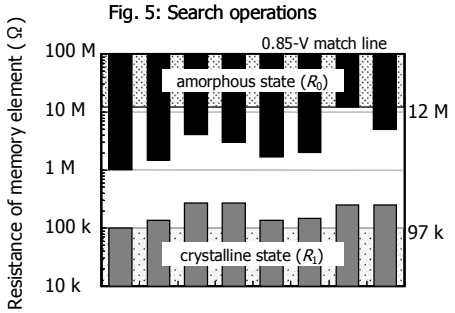
(a) Schematic of memory array

	1st cycle	2nd cycle
Stored data	1000_1000_..._1000	1000_1000_..._1000
Search key (SLs)	1000_1000_..._1011	1000_1000_..._0111
Match line, ML	discharged (I_{ON}+2xI_L)	mid-level (3xI_L: worst)
Operation	matched	unmatched



(b) Simulated waveforms

Fig. 5: Search operations



Condition			1	2	3	4	5	6	7	8
Voltage	VDD	V	1.35	1.35	1.35	1.35	1.65	1.65	1.65	1.65
	VPC	V	0.65	0.65	0.65	0.65	0.75	0.75	0.75	0.75
Temperature		°C	125	125	-40	-40	125	125	-40	-40
MOS model		-	slow	fast	slow	fast	slow	fast	slow	fast

Fig. 6: Required resistances for 8-ns-cycle search operation