

# High-Speed Face Detection in Images with Massive-Parallel Bit-Serial SIMD Processor Using Haar-Like Features

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## 1. Introduction

Recently, several improved processing algorithms for multimedia data, such as JPEG2000, MPEG4, AES, and H.264, have become popular. Furthermore, the needs of face detection are also growing, and it is necessary to process many of these algorithms programmably. These algorithms operate with high quality, and demand a large amount of data processing power. Therefore, in order to execute these algorithms in real time, special-purpose hardware[1] or processors with high clock frequency and large power dissipation must be used. However, special-purpose hardware cannot respond quickly to changes of the algorithm, and that increases cost. A general-purpose processor with high clock frequency, since power consumption is large, cannot be operated in mobile equipment. In order to solve these problems, a Massive-Parallel Bit-Serial SIMD Processor has been reported preciously[2].

In this paper, we report the possibility of high-quality real-time face detection with a Massive-Parallel Bit-Serial SIMD Processor at low power dissipation. We realize this flexible and efficient face detection using Haar-like features, and a cascade of classifiers that can detect also other objects with high accuracy.

## 2. Massive-Parallel Bit-Serial SIMD Processor

The Massive-Parallel Bit-Serial SIMD Processor architecture achieves 17 GOPS for 16 bits additions at 162 MHz clock frequency with only 150 mW power dissipation when implemented in a 90 nm CMOS technology[2]. Fig.1 shows the processor's block diagram, which consists of three main blocks: the SIMD processor core, the controller of the SIMD processor core and the interface module. 1 Mbit SRAM for data registers and 1,024 processing elements (PEs), each for 2 bits in parallel, are connected by a flexible switching network, and are integrated on the small area of 3.1 mm<sup>2</sup> in the 90 nm low-power CMOS process.

Since the Massive-Parallel Bit-Serial SIMD Processor consists of a simple SRAM-based architecture, the processed-data width and the magnitude of parallelism can be changed and optimized with high flexibility according to the needs of each application by software control.

## 3. Effective parallel face detection processing using Massive-Parallel Bit-Serial SIMD Processor

The investigated face detection processing uses a number of Haar-like features arrange in scan windows (SW), and a cascade of classifiers. Therefore, in conventional ASICs or conventional DSPs, the algorithm needs to be processed sequentially as indicated in Fig. 2-(a). On the other hand, with a SIMD processor it becomes possible to process all SWs in vertical direction of the image at once,

as shown in Fig. 2-(b), since all PEs are located in a line and have access to the image data with a 1,024-fold parallelism so that a large improvement in processing speed can be expected. The Haar-like features applied in this investigation use the seven kinds of patterns shown in Fig.3. It detects the faces by changing the position and size of the features used in a SW. For each feature the brightness difference between supposedly black and white areas of the feature are calculated. If the brightness difference is more than a threshold value, it will be judged that the object within the SW agrees with the expected pattern of a face. Therefore, it is possible to suppress changes of light conditions and the influence of image noise, because the relative brightness differences do not change[3]. For efficient and flexible face-detection-algorithm realization with a SIMD Processor, we propose two main methods:

- Image preprocessing with addition and accumulation of the image-pixel data.
- Pointer based parallel processing of the accumulated data at the boundaries of the Haar-like features only.

Generally, there are about 2,000 features in each SW, when open-source data is used[4]. Even if a SIMD Processor is applied, calculating the rectangle brightness difference of features in the straight-forward way takes too much time. Therefore, we investigated the accumulation- addition preprocessing horizontal direction, and stored this accumulated data in the SIMD processor. The brightness differences can then be calculated only from the differences of each rectangular of both ends. Fig.4 illustrates this processing method of the Haar-like features with SIMD Processor resulting in high-speed face detection. Since the horizontal accumulation data is stored, horizontal summation can be realized by specifying both ends of the feature with pointers, and by taking only the difference at these ends. Furthermore, vertical addition and subtraction are carried out by using the vertical data-transfer channel provided in the SIMD processor. For example, horizontal addition is realized by taking the difference of the 0<sup>th</sup> row and the 6<sup>th</sup> row in Fig.4. Vertical calculation is then carried out by addition subtraction of the horizontal sum according the black white regions of the checked feature. With the described methods the SIMD processor achieves a substantial speed-up of the necessary feature evaluation in all SWs, resulting in high-speed face detection.

## 4. Experimental verification with fabricated SIMD processor and evaluation board

We implemented the face-detection procedure on the SIMD processor and verified the performance with an

evaluation board. Fig.5 shows this evaluation board consisting of SIMD processor, Host CPU, DMAC, and main memory. The pictures acquired from mobile devices are stored in the main memory, and the face detection using Haar-like feature is performed by the SIMD processor. The experimental Haar-like features have been determined with a learning algorithm[3] and database of 3,300 faces and 1,500 non-faces, so that all faces could be correctly detected and all non-faces could be correctly rejected. The experimental verification conditions are shown below:

- Picture size for detection : QVGA (320 x 240 pixels)
- Haar-like feature number : 320
- SW sizes: 20 x 20, 24 x 24, 30 x 30, 36 x 36 pixels

For detecting faces larger than 36 x 36 pixels, the SW size is not increased further, but the image is reduced so that the larger faces would fit into 36 x 36 pixels SW.

The total face detection time achieved is about 313 msec at 162 MHz clock frequency of the SIMD processor. For face detection with a digital camera for still pictures this performance is sufficient. Generally, the value of 30 fps is used for the frame rate of video cameras. That means one frame takes the time of about 33 msec. However, when the movement of persons is in a normal range, the position of a face between frames hardly changes. Therefore, it is possible to process the subsequent frames, after initial face detection, only in the vicinity of these faces. Thus the processing load of subsequent frames can be substantially reduced further and we estimate the achieved performance to be sufficient for the video application if the number of faces is not too large.

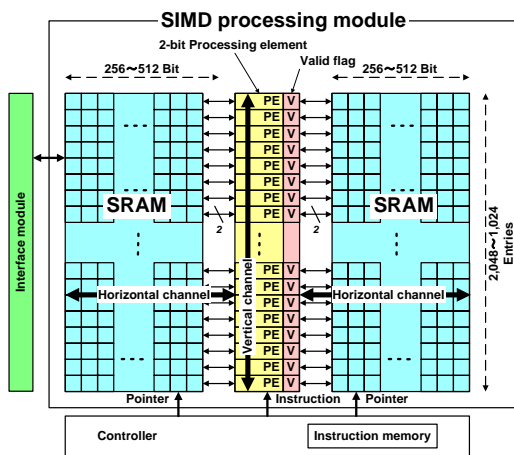


Fig. 1. Block diagram of the Massive-Parallel Bit-Serial SIMD Processor.

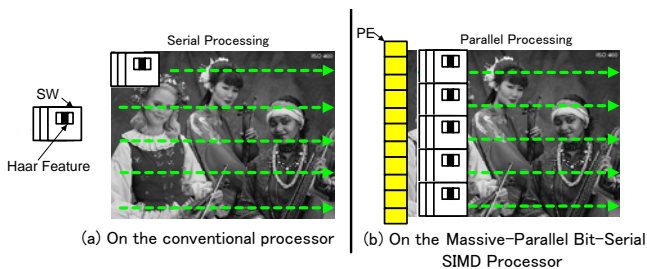


Fig. 2. Processing comparison of a conventional processor and the Massive-Parallel Bit-Serial SIMD Processor.

## 5. Conclusions

In this paper, we reported the possibility of high-quality real-time face detection with a massive-parallel bit-serial SIMD processor at low power dissipation. This offers a processor-base programmable solution for applying Haar-like-feature-based face detection to mobile devices. Furthermore, we verified the high expected face-detection performance experimentally with a fabricated 1,024-parallel, 2 bit-serial SIMD processor mounted to an evaluation board. As a result, the total face detection time is about 313 msec at 162 MHz clock frequency and 150 mW power dissipation. In video applications the processing time per frame is expected to be reducible to below 33 msec, by exploiting the fact that face locations don't move much between frames.

## Acknowledgements

The reported results are obtained as part research collaboration with Renesas Technology Co. We are deeply thankful to M. Tagami, M. Ishizaki, T. Gyoten, H.Noda, Y. Okuno and K. Arimoto of Renesas Technology Co. for their support. Part of this work has also been supported by the 21<sup>st</sup> century COE program and the program "Interdisciplinary Research on Integration of Semiconductor and Biotechnology" for "Creation of Innovation Centers for Advanced Interdisciplinary Research Area", MEXT, Japanese government.

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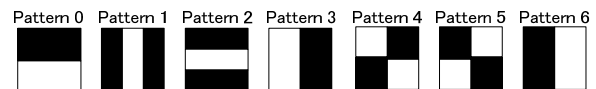


Fig. 3. Used types of Haar-like features.

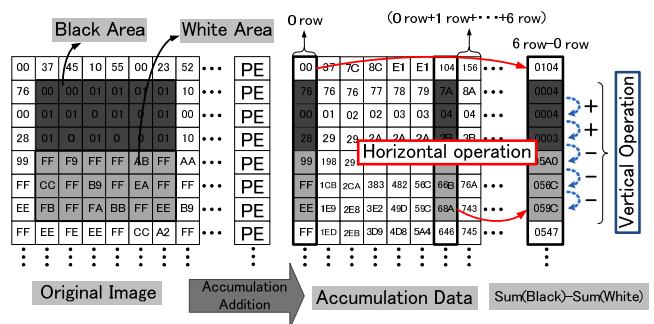


Fig. 4. The Processing method of Haar features with the Massive-Parallel Bit-Serial SIMD Processor.

## Evaluation-Board Architecture

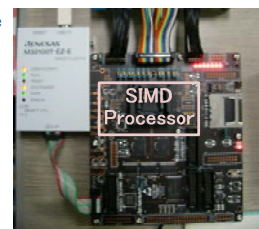
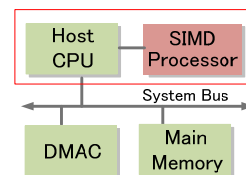


Fig. 5. Architecture and picture of the used evaluation board.