# RF Signal Generator Based on Time-to-Analog Converter in 0.18µm CMOS

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## 1. Introduction

CMOS technology scaling has made it possible to realize digital LSI's with lower power, higher speed, and smaller size at lower cost. However, RF CMOS circuits cannot make use of the scaling effectively because the circuits are analog circuits that use un-scalable devices such as inductors and capacitors, hampering chip area reduction and wideband operation for multi-standard RF systems. Furthermore, lower voltage operation limits the analog performances. To overcome these problems, digital-rich and digitally controllable RF circuit techniques have been studied at laboratories around the globe [1-3].

In this paper, scalable wideband RF signal generator that uses a time-to-analog conversion technique is proposed and confirmed by fabricating the chip using 0.18-µm CMOS.

#### 2. Time-to-analog converter

An extreme solution for RF signal generation is considered to be using high-speed and high-resolution digital-to-analog converters (DAC). To get RF signals with high signal-to-noise ratio of over 50 dB, a resolution of more than 10 bits is required [1]. However, since the lower voltage operation associated with the CMOS technology scaling limits the voltage-domain resolution, pursuing the ordinary voltage-domain DAC performance is expected to become increasingly difficult. We have, therefore, focused on time-domain control, leading to voltages output at irregular time intervals instead of the ordinary voltage-domain control at regular time intervals because circuit speed should improve by scaling. Since the time-domain resolution is expected to become finer with scaling, the circuit is fundamentally scalable and should become wideband.

Figure 1 is a block diagram of the suggested RF signal generator consisting of a multi-tap fine delay circuit, a wave-shape digital controller and a delayed pulse summing circuit. The delay elements could consist of inverters. In the summing circuit, AND gates are used for selection of delayed pulse signals. By summing delayed pulses selected by the waveform digital controller, desired RF signal could be synthesized. If delayed output signals from all delay elements are selected, triangular waveform could be synthesized from rectangular input signal as shown in Fig. 2. If sinusoidal RF signal is desired, delayed signal tap can be selected from the following equation.

$$t_{s}(n) = \left(\sin^{-1}\left(\frac{y_{s+n}}{A}\right)\right) \cdot \frac{1}{2\pi f}$$
(1)

Where ts(n) is the time value; A is the amplitude of the sinusoidal signal; ys is the voltage step; and f is the frequency of the sinusoidal signal. Fig. 3 is a simulation result, when the number of delay elements is 32 (5 bits). The delay  $\tau$  of delay elements is supposed to be 70ps considering the use of 0.18µm CMOS inverters. The sinusoidal frequency is limited to up to 227 MHz.

#### 3. Test chip design of RF signal generator

To confirm the validity of the suggested circuit, two test chips, a triangle signal generator and a sinusoidal generator were designed and fabricated by using a 0.18µm CMOS process. A schematic diagram, common to both test circuits, is shown in Fig. 4. A delay element is composed of two CMOS inverters. The delay is about 70ps. The number of delay elements is 32 (5 bits). To generate sinusoidal RF signal, 26 delayed signals are selected and summed. For triangle generator, all 32 delayed signals are summed. In the chips, waveform digital controller circuit was omitted considering convenience of evaluation. A chip microphotograph of the sinusoidal RF signal generator is shown in Fig. 5.

#### 4. Measurements and discussions

Fig.6 shows a measured triangular output signal. Since all 32 (5-bit) delayed signals were summed, 144MHz triangular waveform was observed. The signal swing was 408 mV peak-to-peak.

Fig. 7 shows measured output signal when 128 MHz rectangle signal was input to the sinusoidal waveform generator. Synthesized 128MHz (period T=7.8ns) sinusoidal RF signal was observed. Output signal level was -6.6dBm as shown in Fig.8. The 2nd harmonic was -23dBc and the 3rd harmonic was -37dBc. Compared with the designed value, the actual operation frequency was lower presumably due to layout parasitics.

RF signal frequency can be set higher if  $\tau$  can be reduced by circuit topology or by the use of finer CMOS process technology.

As regards harmonics, higher resolution should also give reductions in the 2nd and 3rd order harmonics.

#### 5. Conclusions

The time-to-analog conversion technique for RF signal generation has been suggested and confirmed by fabricating the chip. The technique could become particularly attractive in the future when CMOS is much faster yet the supply is deep-sub-1V.

## Acknowledgements

This work was partially supported by STARC, NEDO, KAKENHI, MIC.SCOPE, and VDEC in collaboration with Cadence Design Systems, Inc., Agilent Technologies Japan, Ltd., and Mentor Graphics, Inc.

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Fig.4 Test of the RF Signal Generator

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Fig.5 Chip micrograph of the RF Signal Generator





Fig.6 Triangle output waveform at 144MHz

Fig.7 sinusoidal output waveform at 128MHz



Fig.8 Measured output spectrum with the harmonics

Table1 Sinusoidal chip performance

	Sin wave
Frequency [MHz]	128
Output power[dBm]	-6.6
2nd harmonics [dBc]	-23
3rd harmonics [dBc]	-37