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Improved Characteristics of InAlAs/InGaAs MOS-MHEMTs by Using Ozone Water Oxidation Method

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1. Introduction

Over the past years, InAlAs/InGaAs HEMTs have demonstrated high-frequency and low-noise circuit applications. Narrow energy-gap InGaAs compounds usually accompany with low impact-ionization threshold fields for initiating the kink effects. The resulted kink effects will seriously degrade the device characteristics. Recently, many studies [1-4] have been devoted to investigating the gate insulation techniques to effectively suppress the gate leakage currents. This work proposes an InAlAs/InGaAs MOS-MHEMT with an oxide layer treated by using the ozone water at room-temperature under atmospheric pressure. The present cost-effective ozone water method presents a high growth rate, high quality, nm-thickness, low interface trap, and smooth interface oxide on InAlAs layer. Improved device characteristics have been achieved for the proposed InAlAs/InGaAs MOS-MHEMT in comparison with a conventional MHEMT.

2. Device Structure and Fabrication

The studied InAlAs/GaAs MOS-MHEMT was gown by using the molecular beam epitaxy (MBE) technique. Upon the (100)-oriented semi-insulating GaAs substrate, the epitaxial layer structure of the device consists of a 1.5-μm thick graded $In_xAl_{1-x}As$ metamorphic buffer (MB) layer with indium content (x) varying from 0 to 0.55, a 150-nm thick undoped $In_{0.52}Al_{0.48}As$ inverse step-back barrier layer, an inverted Si δ-doped (1×10^{12} cm^{-2}) monolayer, a 5-nm thick undoped $In_{0.52}Al_{0.48}As$ spacer, a 16-nm thick undoped $In_{0.53}Ga_{0.47}As$ channel, a 5-nm thick undoped $In_{0.52}Al_{0.48}As$ spacer layer, a upper Si δ-doping (3×10^{12} cm^{-2}) monolayer, a 15-nm undoped $In_{0.52}Al_{0.48}As$ Schottky layer, and, finally, a 25-nm thick Si-doped (5×10^{18} cm^{-3}) $In_{0.53}Ga_{0.47}As$ capper. Hall measurement was carried out to characterize the two-dimensional electron gas (2DEG) concentration (n_{2DEG}) and the electron mobility (μ_n) under a magnetic field of 5000 G. μ_n and the corresponding n_{2DEG} values were determined to be 9740 cm^2/V-s and 4.11×10^{12} cm^{-2} at 300K.

A standard photolithography, lift-off and rapid thermal annealing (RTA) techniques were employed for the device fabrication, starting with the mesa isolation by using $H_3PO_4/H_2O_2/H_2O$ chemical solution to etch down to the InAlAs buffer. AuGe/Ni alloys were used as the source/drain ohmic contacts, onto which Au was evaporated to reduce the contact resistance after the rapid thermal annealing (RTA) at 400℃ for 60 seconds. Following the deposition of the source/drain electrodes, the gate-recess selective etching was performed to remove the InGaAs cap layer by using the solutions of the citric acid and hydrogen peroxide. Then, the sample was immersed in an ozone water system to perform the oxidation process. With the source/drain electrodes as the etching mask, selective oxidation can be obtained to form thin oxide films upon the exposed surfaces and sidewalls within the recessed InAlAs Schottky layer. Besides, surface passivation between the gate definition region and the source/drain electrodes can also be obtained at the same time. Finally, the metallization of the Pt/Au alloys and lift-off process were conducted to from the gate electrode. Identical processing has been applied to a conventional MHEMT device, except without the ozone water oxidation treatment to provide direct comparisons. The gate dimensions were 1×200 μm^2 with a drain-to-source spacing of 7 μm for the studied MHEMTs.

The oxidation system includes a Welsbach T-816 ozone generator with a H_2O_2 solution, which can be operated at room temperature under the atmospheric pressure. The ozone gas with a concentration of 17.7 p.p.m. was injected into the H_2O_2 solution to form the ozone water. The oxidation rate by employing the ozone water treament is about 3-4 nm/min. The surface roughness of the InAlAs oxide film was characterized by using the atomic force microcopy (AFM).The optimum surface flatness was obtained by immersing the device in the ozone water for 2 minutes at room temperature. Thin oxide film of only about 8.5 nm thickness with superior surface flatness has been obtained.

3. Experimental Results and Discussions

Figure 1 shows the current-voltage characteristics of the studied MOS-MHEMT and conventional HEMT at room temperature. In the saturation region, the drain-source currents of MOS-MHEMT have demonstrated flatter I-V curves than that MHEMT. It is mainly attributed to the relieved kink-effects in the MOS-MHEMT. With identical I_{DS} = 150 mA/mm at V_{DS} = 2 V for both devices, the output conductance (g_d) values were determined to be 8.3 mS/mm

and 32.8 mS/mm for the MOS-MHEMT and the conventional MHEMT. Figure 2 shows the two-terminal gate-drain breakdown characteristics at 300 K for MOS-MHEMT and MHEMT. The two-terminal gate-drain breakdown (turn-on) voltages, defined at $|I_{GD}|$ = 1mA/mm, were found to be -5.8 (0.8) V and -14.9 (2.25) V for MOS-MHEMT and MHEMT. The inset of Fig. 2 showed the SEM picture of the cross section by using the ozone water treatment. The thickness of the oxide layer is about 8.5 nm thick, verified with a SIMS profile. Superior surface flatness is also obtained by using by an atomic force microscope (AFM).

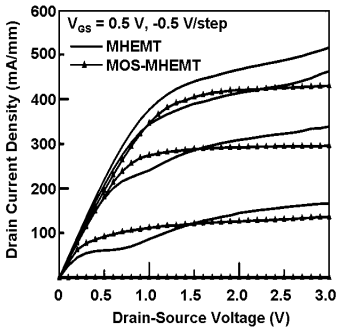

Fig. 1 Common-source current-voltage curves for the studied MOS-MHEMT and conventional HEMT at 300 K.

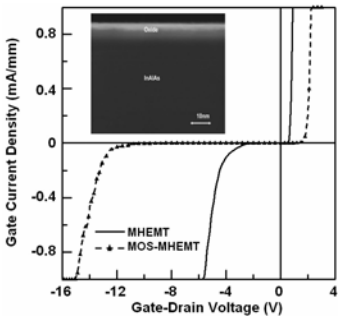

Fig. 2 Two-terminal gate-drain breakdown characteristics at 300 K. The inset shows the SEM photo of the MOS-MHEMT.

Distinguished improvement in the output conductance, breakdown, and turn-on voltages of MOS-MHEMT are due to the decreased surface traps and relieved kink effects by the ozone treatment. Laterally extended depletion region in the channel are resulted from the annihilated screening effects from surface traps, and enhanced barrier height of interfacial discontinuity within the oxide/Schottky layer to obtain relieved impact ionization in the MOS-MHEMT. It is beneficial to the intrinsic voltage gain performance. The cut-off frequency (f_t) and the maximum oscillation frequency (f_{max}) are 27.8 (32) GHz, and 71.3 (72.6) GHz for the MOS- (conventional) MHEMT was shown in Fig. 3. Better high-frequency characteristics of the conventional MHEMT are owing to its higher g_m value. Figure 4 shows the P_{out} and P.A.E. characteristics versus the input power of the studied devices operated at 5.8 GHz. Improved power performances of the MOS-MHMET are mainly due to the improved GVS linearity and gate isolation capability. The MOS-MHEMT (MHEMT) has demonstrated superior P_{SAT} of 18.5 (13.38) dBm and P.A.E of 47.5 (25.8) %.

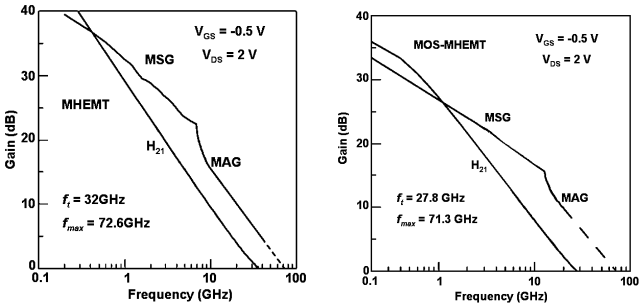

Fig. 3 Microwave characteristics for the studied devices at 300 K.

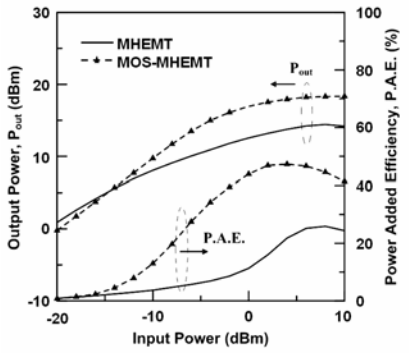

Fig. 4 P_{out} and P.A.E. characteristics versus the input power for the studied devices at 5.8 GHz.

4. Conclusion

In summary the proposed cost-effective ozone water-treated MOS-MHEMT has demonstrated. High layer quality and low interface density with nm-scaled thickness oxide was formed on the Schottky contact layer of the proposed device to effectively suppress the kink effects and decrease the gate leakages. The present device MOS-MHEMT is promisingly suitable for high-gain and high-power MMIC applications.

Acknowledgements

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References

[1] K. W. Lee, N. Y. Yang, M. P. Hong, and Y. H. Wang, Appl. Phys. Lett. **87** (2005) 263501

[2] M. Takebe, K. Nakamura, N.C. Paul, K. Iiyama, and S. Takamiya, IEEE Tran. Electron Device **51** (2004) 311

[3] C. B. Demclo, D. C. Hall, G. L. Snider, D. Xu, G. Kramer, and N. E. Zein, J. Appl. Phys. **36** (2000) 84

[4] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, M. Hong, K.K. Ng, and J. Bude, Appl. Phys. Lett. **84** (2004) 434

[5] A. Mazzanti, G. Verzellesi, G. Sozzi, R. Menozzi, C. Lanzieri, and C. Canali, IEEE Trans. Device and Materials Reliability **2** (2002) 65