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Width Dependent electrically stress Degradation of Bottom Gate Amorphous Indium Gallium Zinc Oxide Thin Film Transistors

Dong-Ho Nam[1], Kwang-il Chai[1], Sung-Soo Park[1], Jeong-Gyu Park[1], Ho-jin Yun[1], Won-Ho Choi[1], Hi-Deok Lee[1], and Ga-Won Lee[1]

[1] Dept. of Electronic Engineering, Chungnam National University, YuSeong, Daejeon 305-764, Korea

Phone: +82-42-821-5666 E-mail: gawon@cnu.ac.kr

1. Introduction

Recently, a-IGZO based thin film transistors (TFTs) have been studied extensively due to their potential to replace a-Si:H or poly-Si TFTs, which have been served in active-matrix organic light-emitting diode (AMOLED) displays. Recent experimental results demonstrated that a-IGZO TFTs present higher carrier mobility and better stability compared with their amorphous silicon (a-Si:H) counterparts, suggesting that a-IGZO TFTs are potentially better candidates as pixel drivers in AMOLED displays[1.2]. AMOLED pixels operate under dc bias, and the OLED current depends on the TFT threshold voltage, the OLED current supplied by the a-IGZO TFT and, thus, the pixel brightness will be degraded as the threshold voltage changes. Therefore, a major technical issue associated with a-IGZO TFTs in AMOLED displays is their electrical stability under dc bias operation conditions.

The aim of this letter is to correlate the width dependent performance with the stability of electrically stressed a-IGZO TFTs.

2. Device structure and Experiments

The experimental structures for this work are n-type a-IGZO TFT with the bottom gate and top contact. MoW (200nm) was deposited as a gate metal and patterned by photolithograpy on a SiO2/glass substrate. Then, SiNx (200nm) film was deposited by plasma enhanced chemical vapor deposition as a gate insulator. Subsequently, the a-IGZO film with a thickness of 50nm was grown by sputtering, using a polycrystalline InGaZnO target at room temperature. During sputtering, the Ar/O2 gas mixing ratio, input power density, and chamber pressure for DC were 72/28, 2.0 W/cm^2, and 3.4 mTorr respectively. After defining the a-IGZO channel using wet etching, a P.A(Poly acrylic) etch stopper was deposited by PECVD and then, patterned by dry. MoW source and drain electrodes (200nm) were formed by sputtering and patterned by dry etching. Finally, the sample was subjected to thermal annealing at 350°C for 1hr. The transfer characteristics of the a-IGZO TFTs were evaluated with an Agilent 4156C precision semiconductor parameter analyzer.

The fabricated TFTs have channel length L = 10 μm and channel width W varying from 10 to 1000 μm. The stability of the a-IGZO test devices is investigated under static bias stress conditions by applying on the gate and drain electrodes the voltages of $V_G = V_D = 20$ V, at room temperature.

3. Results and discussion

The schematic cross section of the fabricated a-IGZO TFTs with inverted staggered bottom gate is shown in Fig. 1 .

Figures 2 shows the transfer characteristics of typical wide(W = 1000 μm) and narrow (W = 10 μm) channel width TFTs, measured before stress and after stress ($V_G = V_D = 20$ V) 10^3 s. It is apparent that the electrical stress is followed by a severe positive V_{on} shift I_{on} degradation for the wide device, whereas these degradation phenomena become weak with shrinking the channel width down to 10μm.

Figure 3 shows the deviation of the initial threshold voltage ΔV_T, extracted after each stress cycle, for devices with different channel widths. We observe that the stressing time at which each device exhibits the positive onset of ΔV_T, occurs earlier for wider devices than for narrower ones.

Figure 4 shows the evolution with stress time of the normalized turn-on voltage $V_{on}/V_{on,o}$, where $V_{on,o}$ is the turn-on voltage before stress. The turn-on voltage V_{on} is extracted from the interceptation the horizontal axis of the linear extrapolation of the I_D–V_G curve. It seems that the electrical stress leads to an initial V_{on} positive shift that becomes more pronounced for wider channel devices. The initial positive V_{on} shift can be attribute to electron trapping in gate insulator and interface traps. These negative charges, assumed to be located at the SiNx/channel interface, are added to the fixed charges in the insulator and thereby shifting V_{on}. V_{on} is shifted faster following a power time dependent of the form: $V_{on}/V_{on,o} = A_1 t^{n1}$ with $n_1 \approx 0.04$. The logarithmic stressing time dependence of the V_{on} shift indicates charge trapping into the gate insulator or at the interface [3]. The prepower law factor A_1 of the V_{on} shift represents the magnitude of the stress-induced V_{on} degradation. From Fig. 5, it is evident that the V_{on} degradation becomes less prominent in narrower channel devices. When the TFTs are subjected to high fields, their temperature is increased by Joule heat[4]. Due to the self heating effects, the electrons acquire higher thermal velocity in wider devices during stressing; as a result, the injection to gate insulater can be accelerated, resulting in larger V_{on} shift[5]. In wider devices, heat disappearance is expected to be reduced.

Figure 6 shows comparison of $\triangle V_T$ of the various temperature condition. Device degradation is more pronounced for high temperature.

Figure 7 shows the variation with stress time of the normalized ON-state current $I_{on}/I_{on,o}$, where $I_{on,o}$ is the drain current before stress and I_{on} is the drain current after stress, for

TFTs with channel widths W = 10, 20, 30, 40, 100, and 1000 μm. I_{on} measured at V_G - V_T= 20 V were used in order to monitor the device degradation. As the stress proceeds, the ON-state current is reduced obeying a power time-dependent law of the form $I_{on}/I_{on,o} \sim t^{-n2}$, where the power-time index n_2 attains higher values with increasing the channel width as shown in Fig. 8. The observed ON-state current degradation can be mainly attributed to the increase of the interface and phonon scattering[6,7].

Figure 9 demonstrates the subthreshold slope variation, extracted after each stress cycle for devices with different channel widths. Under positive bias stress, electrons are attracted toward the interfacial region and captured in interface trap states. Which can be accellerated in high temperature. This results in a temporary fixed negative charge, which causes changes in the band bending and charge distribution in the channel region. In effect, a proportion of electron traps in the channel that are occupied at equilibrium in an as-deposited device is emptied, leading to an increase in the effective density of these trap states in the channel[8]. We observe a continuous increase of the subthreshold slope with increasing stress time for all devices. This increase is more pronounced for wider devices. Hardly variation of subthreshold slope is observed in width less than 20μm. Therefore we can determine that channel width more than 30μm shows self heating effect.

4. Conclusions

In this letter, the stability of a-IGZO TFTs with channel length L = 10 μm and channel width W varying from 10 to 1000 μm has been investigated. From measurements, We observed that the channel width of a device affects its behavior under the application of electrical stress and that the device degradation is more pronounced in wider devices.

We propose that channel width increases degradation of TFTs which is raised up due to self-heating effect and charge taping.

Acknowledgement

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References

[1] Wantae Lim, et. al, APL, 93, 082102(2008). [2] Jae Kyeong Jeong, et. al, APL, 91, 113505(2007). [3] Y.-H. Tai, et. al, APL, vol. 67, no. 1(1995). [4] G.P. Kontogiannopoulos, et. al, MIEL, 11-14 MAY(2008). [5] Ilias Pappas, et. al, EDL. 29, NO. 8, AUGUST(2008). [6] Ilias Pappas, et. al, EDL, vol.29, no. 8, august(2008). [7] M. Alvaro, et. al,ME, 36, 732–736(2005). [8] R. B. M. Cross, et. al, TED vol. 55, no. 5, may(2008)

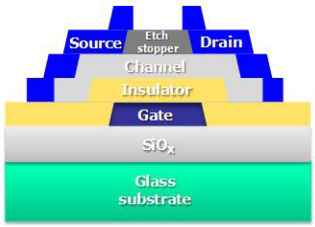

Fig. 1. Schematic cross section of a-IGZO TFTs on glass substrate with bottom gate and top contact structures.

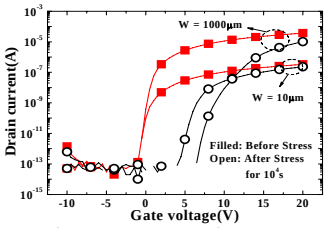

Fig. 2. Transfer characteristics of a-IGZO TFTs with channel length = 10 μm and channel widths W = 10 and 1000 μm. The characteristics were measured at V_D = 0.1 V before and after stress at V_G = V_D = 20 V for 10^3 s.

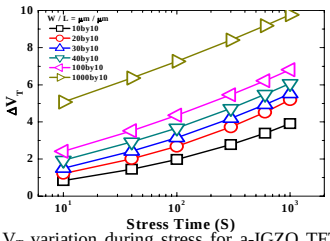

Fig. 3. V_T variation during stress for a-IGZO TFTs with various channel widths. Stress condition: V_G = V_D = 20 V. The V_T was defined by the gate voltage which induces a drain current of W/L×10 nA at V_{DS} of 5.1 V.

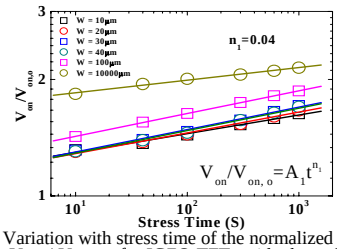

Fig. 4. Variation with stress time of the normalized turn-on voltage Von / Von,o of a-IGZO TFTs with channel length L = 10 μm and channel widths W = 10, 20, 30, 40, 100 and 1000 μm at V_G = V_D = 20 V. V_{on} is extracted from the interceptation the horizontal axis of the linear extrapolation

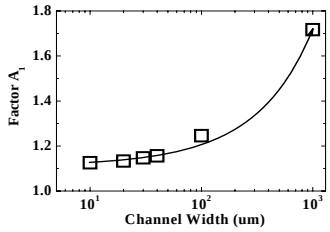

Fig. 5. Extracted values of the prepower law factor A_1 for devices of various channel widths.

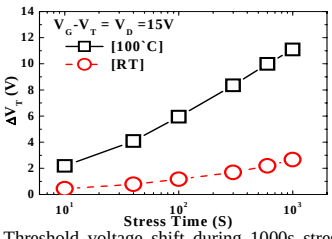

Fig. 6. Threshold voltage shift during 1000s stress time following various temperature condition.

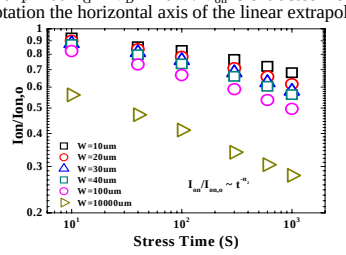

Fig. 7. Variation with stress time of the normalized ON-state current $I_{on}/I_{on,o}$ of a-IGZO TFTs with channel length L = 10 μm and channel widths W = 10, 20, 30, 40, 100 and 1000 μm at V_G = V_D = 20 V. I_{on} measured at V_G-V_T= 20 V

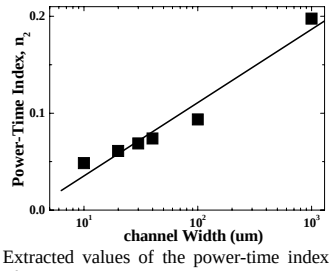

Fig. 8. Extracted values of the power-time index n2 for devices of various channel widths.

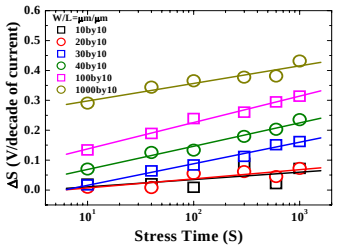

Fig. 9. Subthreshold slop variation during stress for a-IGZO TFTs with various channel widths. Stress condition: V_G = V_D = 20 V