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Low Leakage AlGaN/GaN HEMTs with a High On/Off Current Ratio

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1. Introduction

High performance AlGaN/GaN high electron mobility transistors (HEMTs) have been successfully demonstrated for high power applications in recent years. However, the relatively high Schottky gate leakage current is still a critical issue, which causes an additional noise source [1], collapse effect [2], and device reliability problems [3]. For power electronic applications, a large leakage current also causes additional off-state loss in the power supply and reduces the efficiency of the system.

The leakage sources of HEMTs may originate from surface charge, process induced damage, and bulk/buffer related traps. Several approaches have been adopted to solve the problem. The most straightforward approach is probably the use of an additional gate dielectric to block the leakage current path [4]-[5]. Using the fluoride plasma was also suggested to reduce the leakage current [6]. In this work, we propose a filled-oxide structure to reduce the leakage current, in which the mesa area is fully surrounded by Silicon dioxide. By this approach, the traps around the mesa edge can be alleviated and the gate metal contact across the damaged mesa area can be prevented. In addition, the post gate annealing under an N_2/H_2 mixture ambient is also used to fill up the traps generated during the mesa etching process. A leakage current as low as 10^{-9}A/mm is obtained and an on/off current ratio up to 10^8 is demonstrated in this work.

2. Device Design and Fabrication

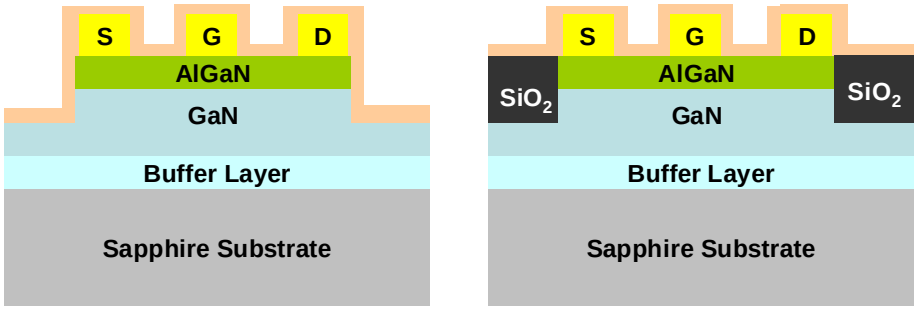
The device structure was grown on a c-plane sapphire substrate by metal-organic chemical vapor deposition (MOCVD). The epitaxial structure consisted of a GaN buffer layer, a 3-μm undoped GaN layer, a 3-nm undoped AlGaN layer, a 20-nm n-doped AlGaN barrier layer, and then followed by a 5-nm undoped AlGaN cap layer. The Al mole fraction in the AlGaN layer was 0.25. The source/drain ohmic contacts were first formed with Ti/Al/Ti/Au (20nm/150nm/45nm/55nm) by rapid thermal annealing at 800 °C for 30 seconds in a N_2 ambient. After the S/D ohmic contact formation, device isolation was achieved by dry etching using Cl_2/Ar gas mixture and the etching depth is about 300 nm. For the filled-oxide structure, a 400 nm-thick e-beam oxide layer was filled around the device active region by lift-off process. Note that the conventional mesa isolation structure without the filled-oxide step is also fabricated for comparison. After the isolation process, the Ni/Au contact (20nm/300nm) was deposited to form the Schottky gate by lift-off process. Following the Schottky gate formation, both samples were annealed at 350°C for 60 seconds in N_2/H_2 ambient for post-gate annealing. A PECVD silicon nitride/silicon dioxide layer of 0.4μm/0.8μm was then deposited for surface passivation. Finally, the pads were opened by RIE using a CHF_3/O_2 mixture. The gate length L_g, the gate to drain spacing L_{gd}, and the gate to source spacing L_{gs} are all 2 μm and the overall widths of both devices are 50 μm. The cross sections of the traditional mesa isolation structure, and the proposed filled-oxide isolation structure are shown in Fig. 1(a) and 1(b), respectively.

3. Results and Discussion

An Excellent on/off current ratio was achieved for each device in this work. Fig.2 compares the I_D-V_G curves of both the conventional and the filled-oxide devices. The on/off ratios of the mesa-isolated and filled-oxide-isolated devices with post-gate annealing are 5×10^6, and 1.2×10^8, respectively, which are greatly improved compared with that of the traditional mesa-type devices without the forming gas treatment (typical on/off ratio of 10^3~10^5) [7]. The results also show excellent pinch off characteristics in this work. The off-state drain leakage currents shown in Fig. 2 are smaller than 10^{-7} A/mm and 10^{-9} A/mm, respectively (typical off-state I_D is 10^{-4}~10^{-6} A/mm for traditional structure). The gate leakage characteristics were also measured as shown in Fig. 3, which is smaller than 10^{-7}A/mm for the mesa isolation and 10^{-9}A/mm for the filled-oxide isolation structures, respectively. Compared with previous studies [7], the gate leakage is much smaller and is even comparable with the device using the MOS-HEMT structure [8]. The probable reason is that the H^+ introduced from the post-annealing can fill up the surface states/traps due to the etching process damage. Fig. 4 shows the measured breakdown voltage of both devices. The off-state drain-to-source breakdown voltage of GaN HEMT with mesa isolated structure is up to 220 V, while the breakdown voltage of GaN HEMT with filled-oxide isolation method is only 130 V (defined as I_{off} = 1mA/mm). The main reason may be attributed to the relative poor quality of e-beam oxide. This point is confirmed by testing the breakdown voltage of a vertical metal-insulator-metal (MIM) diode with 0.4μm-thick e-beam oxide. The measured breakdown voltage of the MIM diode is only 60 V and the calculated critical field is only ~ 1.5 MV/cm, which is much lower than the expected value of 5 MV/cm. The problem of poor-quality oxide caused breakdown voltage degradation may be solved by using PECVD oxide instead of the e-beam oxide layer in future work.

4. Conclusion

In this study, the AlGaN/GaN HEMTs with the filled-oxide structure was proposed to reduce the device leakage current successfully. In addition, the post-gate annealing treatment was also employed to further alleviate the surface states/traps in the transistor. The results showed good on/off ratio and extremely small leakage current for the filled-oxide-isolated devices.



(a) (b)

Fig. 1. AlGaN/GaN HEMTs: (a) mesa isolation structure (b) filled-oxide isolation structure.

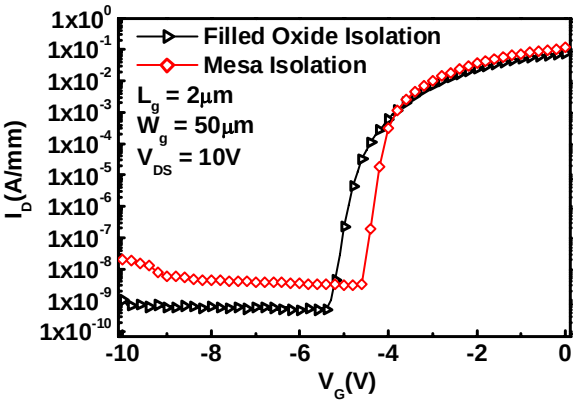


Fig. 2. Measured I_D-V_G characteristics.

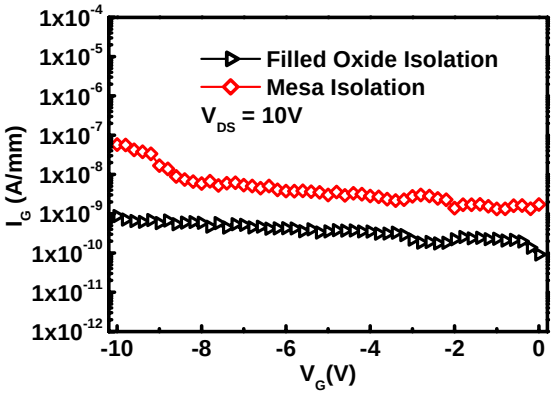


Fig. 3. Measured I_G-V_G characteristics.

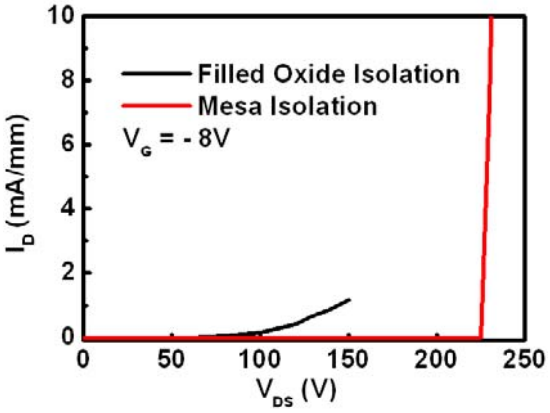


Fig. 4. Measured off-state breakdown characteristics

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