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Silicon Lateral Avalanche Photodiodes Fabricated by Standard 0.18 μm Complementary Metal-Oxide-Semiconductor Process

Koichi Iiyama[1], Hideki Takamatsu[1], Takeo Maruyama[1]

[1]Kanazawa University, School of Electrical and Computer Engineering
Kakuma-machi, Kanazawa, Ishikawa 920-1192, Japan
Phone: +81-76-234-4887 E-mail: iiyama@t.kanazawa-u.ac.jp

1. Introduction

Data transmission speed in electronic systems can be enhanced by utilizing optical transmission technique, and the optical transmission has been studied in board-to-board and chip-to-chip data transmission. In these applications, short wavelength vertical cavity surface emitting lasers (VCSELs) and Si photodiodes (PDs) are used for low-cost system configuration. Si PDs fabricated by complementary metal-oxide-semiconductor (CMOS) process are expected for monolithic integration with transimpedance amplifiers, limiting amplifiers and following electronic circuits. Fast PDs fabricated by CMOS process using bulk Si have the responsivity of about 0.04 A/W and the bandwidth of about 1 GHz at 850 nm [1,2]. In these PDs, the photocurrent generated in the substrate is canceled by differential configuration consisting of an illuminated and a shaded PDs. As a result, the bandwidth is increased at the sacrifice of the responsivity. The bandwidth can be increased to 10 GHz by using a silicon-on-insulator (SOI) substrate [3,4], and the responsivity is, however, 0.08 A/W because of the thin Si layer. Recently, avalanche photodiodes (APDs) fabricated by standard CMOS process are reported [5,6], and the avalanche gain is, however, less than 5.

In this paper, we report a Si APD fabricated by standard 0.18 μm CMOS process. The APD has the maximum avalanche gain of 224 with 800 MHz bandwidth.

2. Structure

Figure 1 shows the schematic structure of the APD by standard 0.18 μm CMOS process, which was fabricated in Rohm Corporation in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo. The thickness and the doping concentration of the n-well, the n^+-layer and the p^+-layer are not disclosed. The light is illuminated from the top of the APD. When the APD is reverse biased, the n-well is depleted and the photogenerated carries generated in the n-well is drifted toward the n^+- and the p^+-layers, and then extracted as a photocurrent. However, the depth of the n-well in CMOS process is very shallow (typically 1~2 μm), and the most of the illuminated light is penetrated into the p-substrate. The features of our APD are as follows.

1. In conventional CMOS process, silicides are formed on the n^+- and the p^+-layers to achieve low contact resistance with metal electrodes. In the CMOS process we utilized, silicides can be formed on a portion of the n^+- and the p^+-layers, and then silicide-free n^+- and the p^+-layers can be obtained. Since silicides absorb light, the silicide-free region is useful for efficient photodetection.
2. The n^+-layers in the n-well and the p^+-layers outside the n-well are electrically connected to cancel the photogenerated carries generated in the p-substrate. The photo-generated holes and electrons generated in the p-substrate are collected by the p^+-layers outside the n-well and the n^+-layer in the n-well, respectively, and then the holes and the electrons are recombined and are not contributed to the photocurrent.

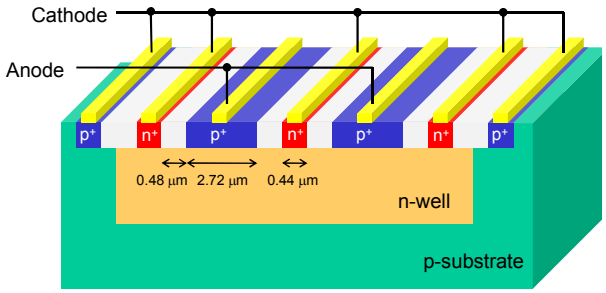

Fig. 1: Schematic structure of the fabricated APD.

The silicide widths for the n^+- and the p^+-layers are 0.44 μm and 0.72 μm, respectively, which are the minimum width determined by process. Between the n^+- and the p^+-layers, 0.48 μm-wide oxide regions are formed for electrical isolation. The width of the silicide-free p^+-layers is 2 μm. The detection area is 20 x 20 μm^2.

3. Characterization

Figure 2 shows the measured I-V characteristics with and without the optical illumination. The wavelength of the illuminated light is 650 nm. The dark current is about 3 nA, and is drastically increased when the bias is about 8 V; about 9 nA at 8 V bias and more than 1 mA at 8.1 V bias; which means the breakdown voltage is 8.1 V. In Si pn diodes, when the breakdown voltage is larger than $6E_g/q$ = 6.7 V, the breakdown is caused by avalanche mechanism, and then the breakdown of the APD is caused by avalanche mechanism. Under light illumination, the photocurrent is almost constant when the bias is below 4 V, and is gradually increased, especially when the bias is above 6 V. For example, the photocurrent near 8 V bias is about 100 times larger than that at low bias region without increasing the dark current. The extreme current increase is due to

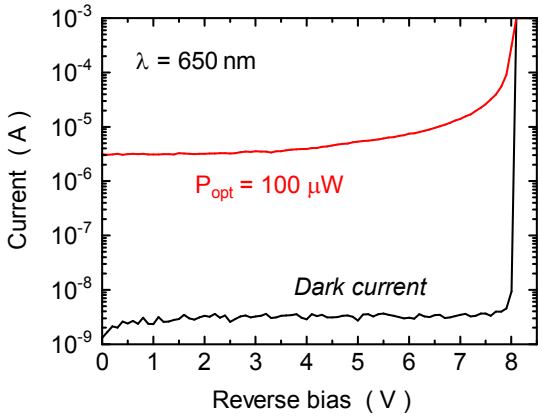

Fig. 2: Measured I-V characteristics. The wavelength of the illuminated light was 650 nm.

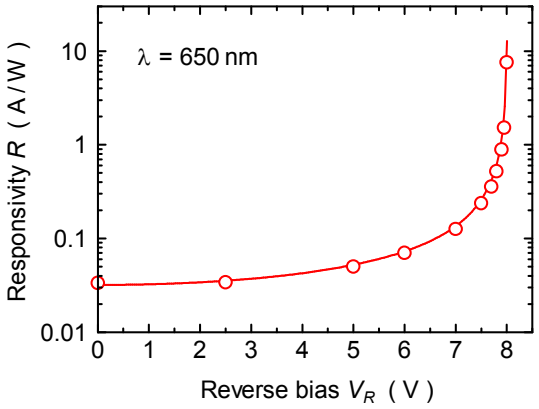

Fig. 3: Responsivity against the reverse bias voltage.

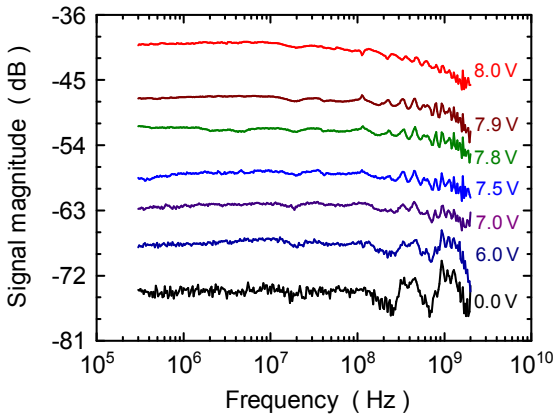

Fig. 4: Measured frequency response for various reverse bias voltage.

avalanche amplification below the p^+-layers in the n-well.

Figure 3 shows the responsivity against the bias voltage at 650 nm wavelength. The responsivity was derived from the photocurrent change against the illuminated optical power below 10 μW to avoid nonlinear photocurrent change. The open circles are the measured results. The responsivity in low bias region is 0.034 A/W, which is lower than that of commercial Si photodiodes (typically 0.4 A/W at 650 nm wavelength). One reason is that about 30% of the Si surface is covered by the silicides for electrode forming, and the other is due to the cancellation of photogenerated carries generated in the p-substrate. The responsivity is increased with the bias voltage, and is 7.6 A/W at 8 V bias voltage, showing the avalanche gain be 224. It is worth noting that the large avalanche gain is obtained at only 8 V bias, in contrast with the commercial APD (typically 150 V).

In APDs, the responsivity R is well described by;

$$R = \frac{R_0}{1 - |V_R / V_B|^n}$$

where R_0 is the responsivity at a low-bias voltage, V_R is the reverse bias voltage, V_B is the breakdown voltage, and n is the integer. The solid line in Fig. 3 is obtained by using the above equation with $n = 2$.

Figure 4 shows the measured frequency response of the APD. The measurement bandwidth was about 2 GHz due to limitation of the laser source. For the bias below 7.9 V, the 3 dB bandwidth is almost unchanged and is 1.6 GHz. The 3 dB bandwidth at 8.0 V bias is decreased to 800 MHz, which is due to multiplication time in avalanche amplification occurred in large avalanche gain.

4. Conclusions

In conclusion, a Si APD was fabricated by standard 0.18 μm CMOS process, and was characterized. The APD has interdigital electrode structure, and the silicide-free p^+-layers are used for efficient optical absorption. At 650 nm wavelength, the responsivity is 0.034 A/W in low bias region, and is increased to 7.6 A/W at only 8 V bias due to avalanche amplification, and the resultant maximum avalanche gain was 224. The bandwidth was 1.6 GHz at low bias region and 800 MHz for large avalanche region.

Acknowledgements

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