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The Drivability Enhancement of Poly-Si TFTs by use of Nanograting Substrate

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1. Introduction

Poly-Si thin film transistors (Poly-Si TFT) have been widely used in active-matrix liquid crystal display (AM-LCD) technologies. For the high aperture ratio of LCDs, the enhancement of the current drivability of TFTs is needed. The nanograting channel structure was effective to enhance the current drivability of MOSFETs [1]. The nanograting channels increased not only the effective channel width but effective carrier mobilities due to strain effect in the channel.

In this work, the nanograting channel structure was firstly introduced to Poly-Si TFT for enhancing its current drivability.

2. Experiments

The nanograting channel Poly Si TFTs were fabricated as follows. Figure 1 shows the schematics of nanogrationg TFT. The processes for the fabrication of the nanograting substrates are shown in Fig. 2. The Si substrates were oxidized at temperature of 1050ºC for 2 h. The thickness of the oxide was 600 nm. Si_3N_4 film with the thickness of 20 nm was deposited by LPCVD at the temperature of 800ºC. After the deposition of Si_3N_4 film, APCVD oxide film was deposited by using SiH_4 and O_2 gases at the temperature of 400ºC. After the deposition of APCVD SiO_2, the samples were annealed at the temperature of 800ºC for 2 h. The thickness of the annealed APCVD oxide film was 600 nm. The upper oxide layer was patterned into line and space with different dimensions. The etching of upper SiO_2 layer was carried out by a RIE at the power of 100 W, with a CF_4-H_2 etching gas. After the formation of trench patterns in the upper oxide, amorphous silicon was deposited with the thickness of 150 nm by LPCVD. The fabrication processes of nanograting TFTs were shown in Fig. 3. The fabricated nanograting substrates for TFT were crystallized by solid phase crystallization (SPC) at the temperature of 650°C for 6 h. By using the crystallized nanograting substrates, n-channel poly-Si TFTs were fabricated. Source and drain regions were formed by P^+ implantation with a dose of 2×10^{15} cm^{-2} and an acceleration energy of 25 keV and activation annealing in N_2 ambient at 900°C for 2 h. The gate SiO_2 films with the thickness of 200 nm were formed by APCVD and annealing in O_2 ambient at 900°C for 1 h. After the formation of contact holes, gate, source and drain electrodes were formed by Al evaporation. Finally, the samples were sintered in N_2/H_2=90/10 ambient at 400°C for 30 min.

3. Results and Discussions

For the comparison, the typical characteristics of the conventional planar TFTs with the same fabrication processes were measured. Figure 4 shows the I_D-V_{GS} characteristic of a conventional TFT with channel width of 100 μm and length of 20 μm. The transconductance characteristic was also shown. By defining the threshold voltage as the voltage when the drain current was 1 nA/μm in the linear region, the threshold voltage was determined as 12.8 V. The I_D-V_{DS} and I_D-V_{GS} characteristics of the nanograting TFTs were measured by the same bias condition as the case of the planar TFTs. The characteristics of the nanograting TFT with the pitch of the nanogratings of 5 μm were shown in Fig. 5. It was evident that by using the nanograting channel structure, the current drivability of TFT was enhanced. Figure 6 shows the enhancement of channel width which was calculated from the resistance increase in the phosphorus-doped Poly Si film. If the enhancement of effective width is x, the total resistance will be $(1+x)^2$ of that of the planar one. The calculated channel width enhancement was well consistent with that from the SEM observation. Figure 7 shows the enhancement of drain current and capacitance for different nanogrationg pitches. The enhancement of gate channel capacitance was larger than the enhancement of channel width. Since the gate insulator was formed by APCVD, the film at the planar region will grow fast than that at the sidewalls, resulting in the thinner average oxide film in the nanograting TFT. And with the larger pitch, the ratio of the region with thinner oxide film will be smaller, and the enhancement of capacitance will nearly identical to the enhancement of channel width. The drain currents of the nanograting TFTs with different pitch were compared to that of the conventional planar TFT. The enhancement of the current was also calculated as shown in Fig. 7. The enhancement of drain current turned out to be larger than the enhancement of the gate channel capacitance. Figure 8 shows the dependence of carrier mobility on the count of nanogratings in the channel. The carrier mobility in the nanograting TFT increased as the count of the nanogratings in the channel and became 42% larger than that of the planar TFT at the maximum. The more nanogratings in the channel, the higher the carrier mobility. This enhancement was considered to be due to the better Si crystallinity at the nanograting edge and the strain effect.

4. Conclusion

The nanograting TFT was proposed and fabricated by using a SPC poly-Si film. At the same overdrive voltage, the drain current of the nanograting TFTs was larger than that of the conventional planar ones at the same planar dimension. Adding to increase of the channel width and thinner gate insulators of the nanograting TFTs, the drivability enhancement was caused by increase in electron mobilities in the channel due to strain effects. The 42% increase of the electron field effect mobility was experimentally achieved at the maximum.

5. Acknowledgment

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References

[1]. X. Zhu, S. Kuroki, K. Kotani, M. Fukuda, H. Shido, Y. Mishima, and T. Ito, Jpn. J. Appl. Phys. 47, pp. 3081-3085, 2008.

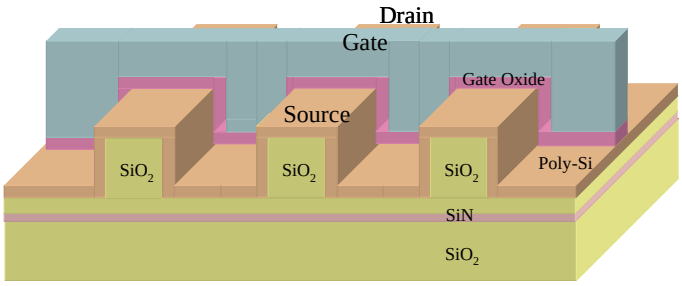

Fig.1 The schematic diagram of nanograting TFT.

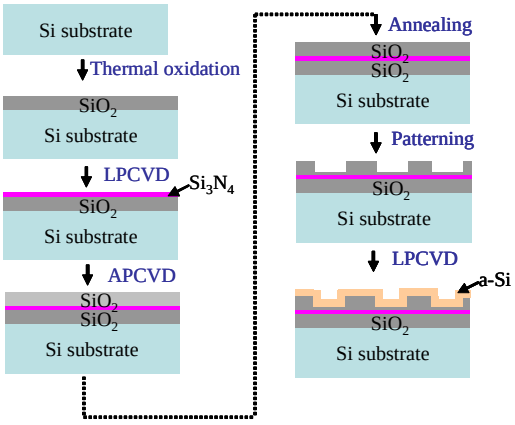

Fig.2 The fabrication processes of nanograting substrate for TFTs.

- Fabrication of nanograting substrates
- Crystallization (650ºC, 6 h、N_2)
- Patterning of active layer
- Formation of dummy gate using resist
- Ion implantation of source/drain region
- Activation annealing (N_2, 900ºC, 2 h)
- Deposition of gate insulator (NSG, 200 nm)
- Annealing of gate insualtor(O_2, 900ºC, 1 h)
- Formation of contact holes
- Evaporation of electrodes (Gate, Source, Drain)
- Sintering

Fig.3 The fabrication processes of nanograting TFTs.

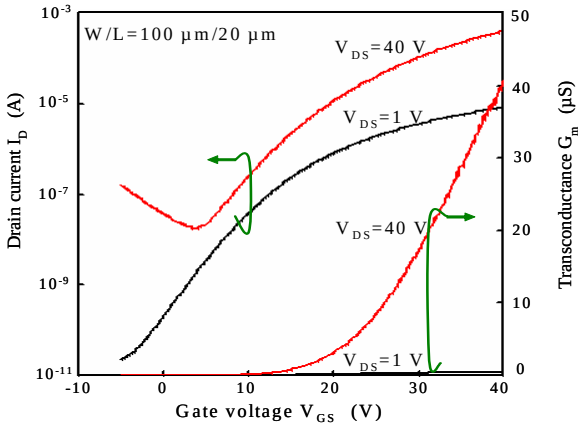

Fig.4 I_D-V_{GS} characteristic of a conventional planar TFT with the channel width of 100 μm and channel length of 20 μm.

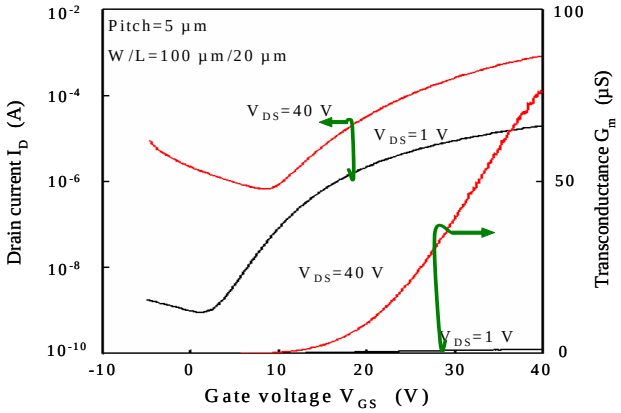

Fig.5 I_D-V_{GS} characteristic of the nanograting TFTs with the planar channel width of 100 μm and channel length of 20 μm.

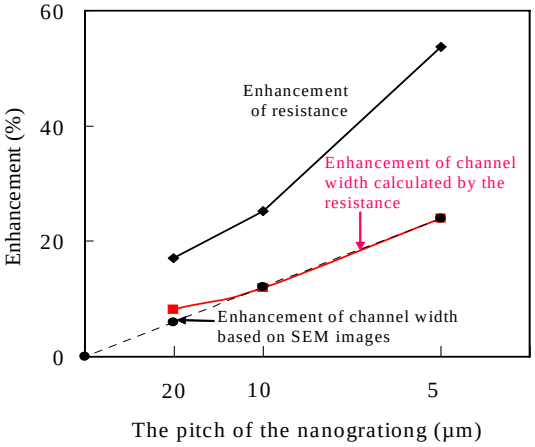

Fig.6 The enhancement of channel width for different nanograting pitches.

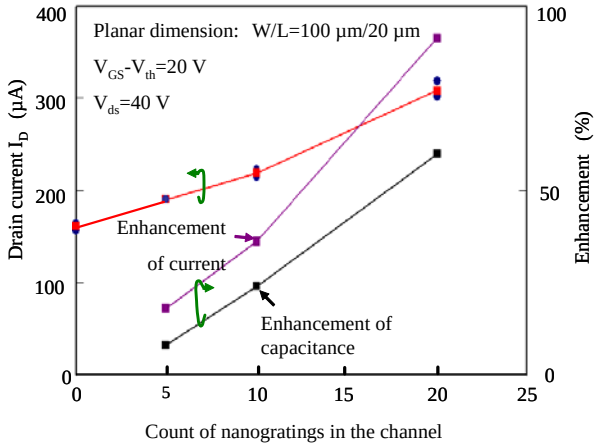

Fig.7 The enhancement of the drain current.

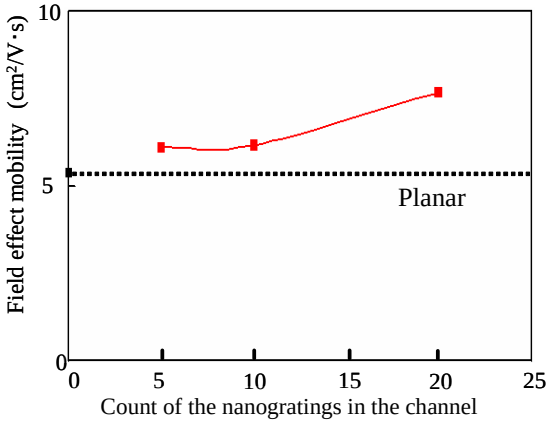

Fig.8 The electron field effect mobility in the nanograting TFTs .