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Comparative Study of Tunnel FETs and MOSFETs for Low-Power Consumption

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1. Introduction

Due to the global energy crisis and the burgeoning demand of portable devices, low-power consumption becomes one of the most important requirements in semiconductor industry. The most efficient way to reduce power consumption is to reduce operation voltage (V_{DD}). However, it is difficult to achieve sub-1-V V_{DD} in the case of metal-oxide-semiconductor field-effect transistors (MOSFETs). It is because the subthreshold swing (SS) value of MOSFETs has a physical limitation of 60 mV/dec at room temperature. As long as thermionic emission is used as a source carrier injection mechanism, the only way to achieve sub-60-mV/dec SS is to lower temperature, which is not applicable to consumer electronics. In order to achieve sub-60-mV/dec SS at room temperature, recently, some novel devices have been proposed [1]-[3]. Among them, we have focused on the tunnel FET [3]. Its basic structure is a gated p-i-n diode as shown in Fig. 1 (a). Since source carriers are injected by band-to-band tunneling instead of thermionic emission as depicted in Fig. 1, the tunnel FET has no physical limit in the SS value. We have confirmed that the TFET can have sub-60-mV/dec SS at room temperature based on the experimental data in previous research [3].

In this paper, the characteristics of tunnel FETs will be compared with that of MOSFETs in terms of SS, ON/OFF current ratio, ON current and OFF current by using simulation results.

2. Simulation and Results

Two-dimensional simulation has been performed by ATLAS simulator [4]. Simulation parameters were carefully adjusted referring to Ref. [3]. Fig. 1 shows the simulated structure of the tunnel FET and the MOSFET. We observed four parameters such as SS, ON/OFF current ratio, ON current and OFF current as a function of the gate oxide thickness (t_{ox}), the silicon-on-insulator (SOI) layer thickness (t_{SOI}) and strain. All four parameters were extracted when the drain voltage is 1 V. The OFF current was defined as the minimal drain current while the ON current was defined as the drain current when the gate voltage increased by 1 V from its OFF state value. The gate length (L_G) was fixed at 70 nm.

Fig. 2 shows the dependence of the four parameters on t_{ox}. As t_{ox} decreases, the SS value is observed to become smaller both in tunnel FETs and MOSFETs. It is because the SS value is determined by two factors: the coupling between the gate voltage and the channel potential and the influence of the drain voltage on the tunneling (tunnel FET) or channel (MOSFET) barrier. As t_{ox} is scaled down, the channel potential becomes more closely coupled to the gate voltage, which leads to decreased SS value. Thus, the SS value of tunnel FETs becomes < 60 mV/dec when t_{ox} is around 2 nm [3]. Also, the ON/OFF current ratio of tunnel FETs is observed to increase more abruptly than that of MOSFETs as t_{ox} becomes smaller. It is because the OFF current of tunnel FETs decreases faster than that of MOSFETs for smaller t_{ox} as shown in Fig. 2 (b). MOSFETs remain in the punch-through mode even when t_{ox} is 2 nm. It proves that tunnel FETs are more immune to short channel effect than MOSFETs.

Fig. 3 shows the dependence of the four parameters on t_{SOI}. It is observed that the performance of MOSFETs is improved faster than that of tunnel FETs since MOSFETs are less affected by short channel effect. However, tunnel FETs exhibit lower SS and higher ON/OFF current ratio than MOSFETs in spite of lower ON current.

Although tunnel FETs exhibit an extremely low SS and OFF current value, considering circuit delay, their ON current should also be improved. Since low ON current stems from the source carrier injection mechanism: band-to-band tunneling, lower bandgap substrate such as strained SOI (SSOI) can be introduced for further improvement in ON current,. Fig. 4 shows the key process flow of an SSOI wafer [5]. We increase x of $Si_{1-x}Ge_x$ from 0 to 0.4 for higher strain in the SSOI layer, which means higher strain and lower bandgap energy. Fig. 5 shows the dependence of the four parameters on x of $Si_{1-x}Ge_x$. Although x increases, the SS values of tunnel FETs and MOSFETs remain almost the same. However, as strain increases, the ON current of tunnel FETs surpasses that of MOSFETs at the sacrifice of ON/OFF current ratio. Since the OFF current increases more abruptly than the ON current as a function of strain, in the case of tunnel FETs, ON/OFF current ratio lowering is inevitable when high ON current is required.

3. Conclusions

Comparative study of tunnel FETs and MOSFETs has been performed in terms of SS, ON/OFF current ratio, OFF current and ON current for low-power consumption. Tunnel FETs exhibit extremely small SS (< 60 mV/dec) and OFF current and good immunity to short channel effect compared with MOSFETs. Although the ON current of tunnel FETs is lower than that of MOSFETs, it is observed that low bandgap substrate such as SSOI can boost the ON current at the sacrifice of ON/OFF current ratio due to rapid OFF current increase. It is expected that the tunnel FET can be a good alternative to the MOSFET for low-power application.

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References

[1] K. Gopalakrishnan *et al.*, *Tech. Dig. of IEDM*, pp. 289-292, 2002. [2] H. Kam *et al.*, *Tech. Dig. of IEDM*, pp. 477-480, 2005. [3] W. Y. Choi *et al.*, *IEEE Elec. Dev. Lett.*, vol. 28, no. 8, pp. 743-745, Aug. 2007. [4] SILVACO International, ATLAS User's Manual. [5] Langdo *et al.*, *IEEE Int. SOI Conf.*, pp. 211-212, 2002.

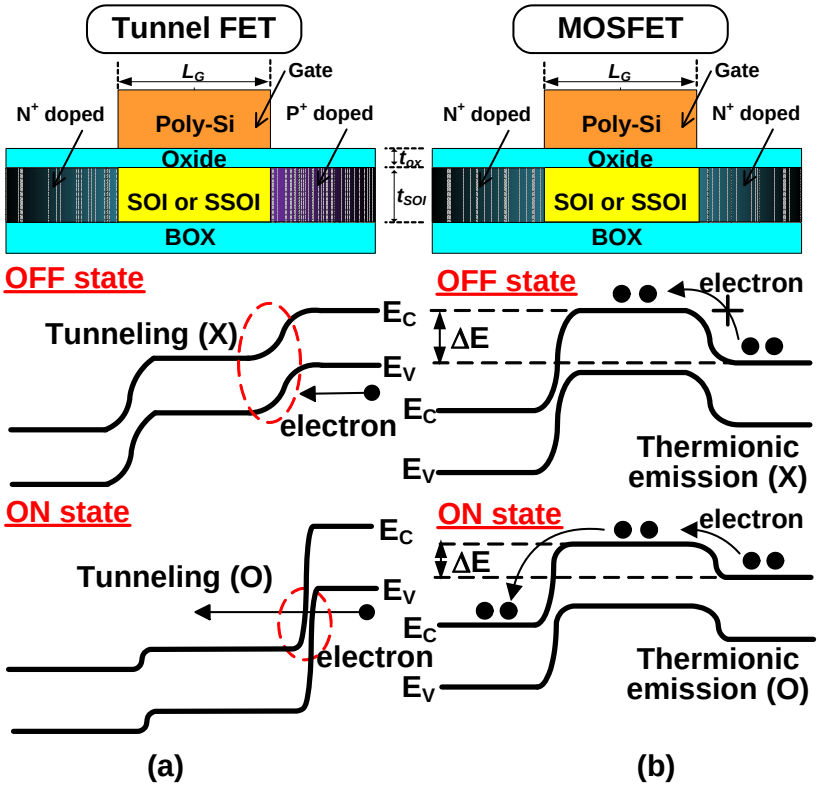

Fig. 1. Schematics and band diagrams of (a) tunnel FET and (b) MOSFET.

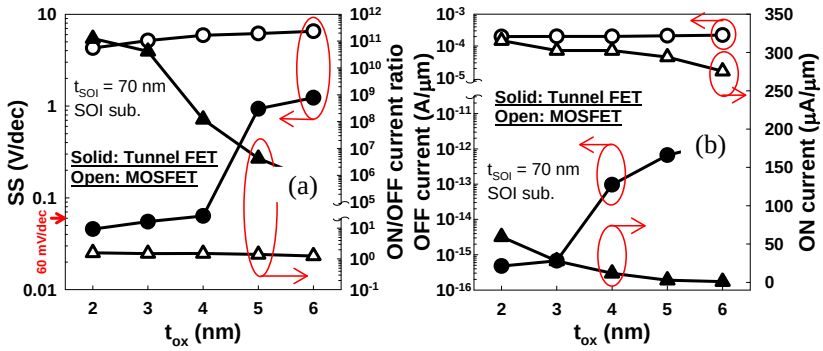

Fig. 2. (a) SS and ON/OFF current ratio of tunnel FETs and MOSFETs with variation of t_{ox}. (b) OFF and ON current of tunnel FETs and MOSFETs with variation of t_{ox}.

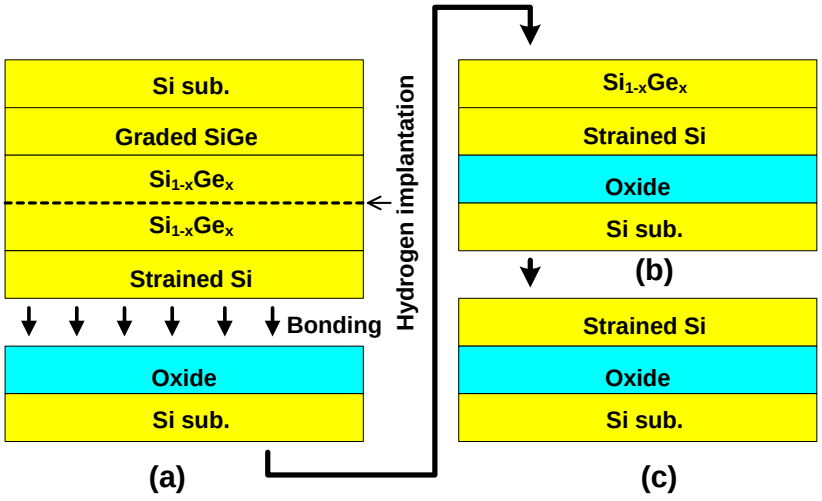

Fig. 4. Key process flow of an SSOI wafer. (a) Hydrogen implantation. (b) Strained Si layer bonding. (c) Removal of strained $Si_{1-x}Ge_x$ layer.

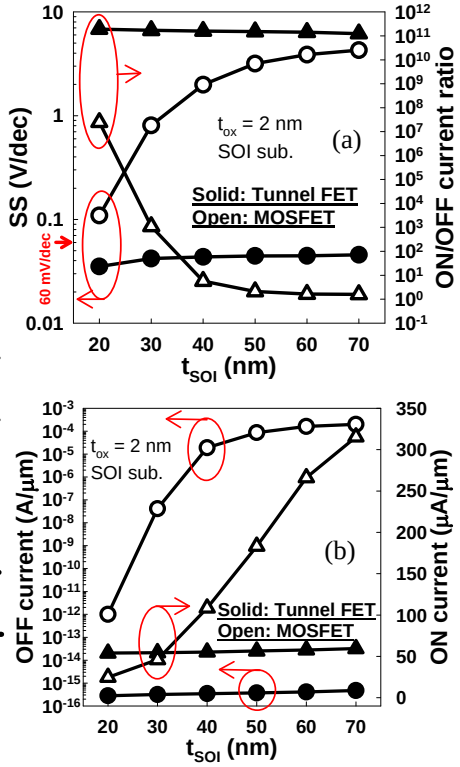

Fig. 3. (a) SS and ON/OFF current ratio of tunnel FETs and MOSFETs with variation of t_{SOI}. (b) OFF and ON current of tunnel FETs and MOSFETs with variation of t_{SOI}.

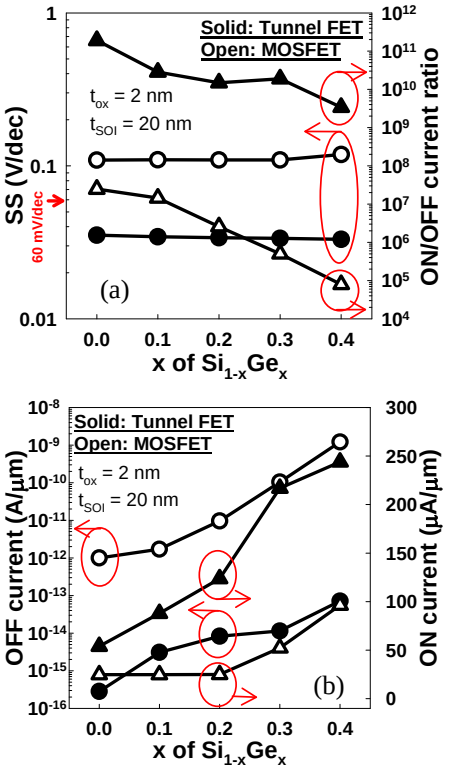

Fig. 5. (a) SS and ON/OFF current ratio of tunnel FETs and MOSFETs with variation of strain. (b) OFF and ON current of tunnel FETs and MOSFETs with variation of strain.