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A Non-local Algorithm for Simulation of Band-to-Band Tunneling in a Heterostructure Tunnel Field-Effect Transistor (TFET)

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Abstract

We report the demonstration of a TCAD simulator with a non-local algorithm for simulating band-to-band tunneling (BTBT) in a heterostructure tunneling field-effect transistor (TFET). A heterostructure TFET (Ge-source Si TFET) with steep sub-threshold swing S (~10 mV/decade) and high I_{on}/I_{off} ratio is investigated and compared with a Ge TFET. The effect of Ge/Si heterojunction position on device performance is also studied.

1. Introduction

The tunneling field-effect transistor (TFET) is a promising device option for possible CMOS replacement. It realizes a steep sub-threshold swing S of less than 60 mV/decade at room temperature so that a high I_{on}/I_{off} ratio can be achieved at low supply voltage V_{DD}. This enables further V_{DD} scaling and reduction in power consumption [1]-[2]. Good TFET design relies on accurate modeling of band-to-band tunneling (BTBT) current, which is an important determinant of its performance. The Kane's model for calculation of BTBT is widely adopted in TCAD simulators [1]. However, this gives limited accuracy in BTBT simulation, especially for heterostructure TFETs. When used in a local model [Fig. 1(a)], generated electron and hole pairs calculated from the generation rate G_{BTBT} are placed locally, which is physically incorrect. There are also issues in its implementation in a non-local model [Fig. 1(b)]. Difficulties also arise in simulating tunneling across a heterojunction where parameters like bandgap E_g at the start and end points of the tunneling path are different.

In this work, we report the demonstration of a TCAD simulator having a non-local algorithm for enabling physics-based BTBT simulation across a heterojunction. Using this simulator, the performance of heterostructure TFET with Ge source, Si channel and drain (Ge-source Si TFET) was studied. Dependence of TFET performance on Ge-Si heterojunction position was also studied.

2. Proposed Simulator and Device Structure

The simulator used in this work introduces a novel non-local algorithm for accurate calculation of the BTBT current across a heterojunction. The simulator captures the essential physics of multi-dimensional tunneling, and is capable of automatically identifying physical tunneling paths in a 2D device structure [4]. A simplified flow chart for this algorithm is summarized in Fig. 2.

The simulator derives the tunneling probability and tunneling current along each path using WKB approximation [5], where each tunneling segment is computed using the local parameters within the respective mesh grids [Fig. 3(a)]. Physics-based modeling contributes to accuracy in BTBT current calculation. To search for the tunneling path, the simulator finds the entire conduction band E_C front and valence band E_V front which are the boundaries of the forbidden region, and the device is discretized in energy scale. Tunneling happens within a small energy range ΔE around E [Fig. 3(b)], the forbidden region between E_C and E_V front is divided into many narrow strips and the tunneling path is generated in each non-overlapping single strip. Fig. 4 demonstrates the simulated tunneling path across heterojunction found by the simulator for a small energy step ΔE. Finally, the total tunneling current is obtained by integration over all energies levels E.

The heterostructure double-gate n-channel TFET simulated here is shown in Fig. 5(a), where the source material is Ge, while Si is used in both channel and drain. Fig. 5(b) shows the contour of the simulated G_{BTBT} for this TFET device. BTBT occurs very near to the surface.

3. Simulation Results and Discussion

The performance of Ge-source Si TFET and all-Ge TFET is compared as shown in Fig. 6. The two devices have the same physical parameters or geometry. Compared to Ge TFET, the heterostructure TFET has better performance. It achieves a lower off-state leakage current I_{off} (~3×10^{-11} mA/μm), higher on-state drain current I_{on} (~0.3 mA/μm), much steeper S (~10 mV/decade) and a smaller threshold voltage V_T (~0.2 V). In TFET operation, tunneling barrier width ω_T is a critical parameter that determines the rate of electron tunneling through the barrier. From the simulated energy band diagram in the off-state [Fig. 7(a)], a wider ω_T at the channel-drain junction of Ge-source Si TFET suppresses the drain side tunneling due to the large E_g of Si (as compared to Ge), which results in a lower I_{off}. In the on-state [Fig. 7(b)], the heterojunction at source side contributes a narrower ω_T (~2.3 nm) compared to that of Ge TFET (~4.2 nm) under the same V_{GS} (~0.6 V), which gives rise to a higher I_{on}. The V_T is defined as the gate voltage at I_{on} of 10^{-4} mA/μm in this work. With the same gate workfunction Φ_M (4 eV) and channel doping, the large E_g of Si in heterostructure TFET results in a more negative V_{FB} and thus a smaller V_T.

To further investigate the behavior of Ge-source Si TFET, the position of Ge/Si heterojunction is varied while the source/drain dopant profile remains the same (Fig. 5). The I_D-V_G plot [Fig. 8(a)] shows that the device has the best performance when the overlap of Ge-source under gate L_{ov} = 0 nm, and the performance degrades when L_{ov} changes either from 0 nm to 5 nm or to -5nm. As the Ge-Si heterojunction is shifted into the channel ($L_{ov} > 0$), the device behaves more like a Ge TFET and the energy band diagrams in Fig. 8(b) reveal that the tunneling region remains in Ge. Similarly, as the Ge/Si heterojunction is moved away from the gate edge ($L_{ov} < 0$), the ω_T at source side becomes even larger since it becomes more like a Si TFET.

4. Conclusion

A TCAD simulator with a non-local algorithm for calculation of BTBT across a heterojunction was developed. Based on this simulator, the *I-V* characteristics of Ge-source Si-channel TFET was investigated. Good device characteristics was obtained, showing a steep S (~10 mV/decade). The device shows superior performance over an all-Ge TFET. Moving the Ge/Si heterojunction position under the gate changes the device behavior towards a Ge TFET, while moving the Ge/Si heterojunction away from the gate makes it more like a Si TFET. The simulator can also be used to design TFETs with novel source heterostructures.

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References

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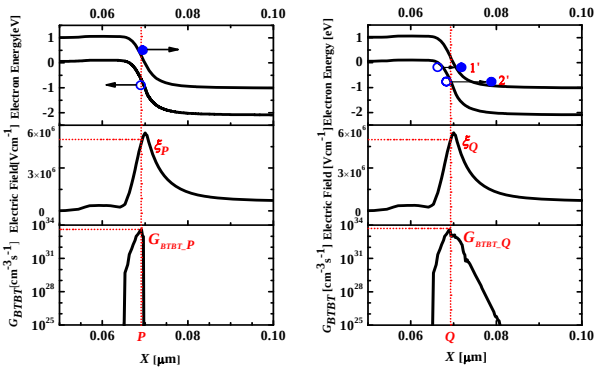


Fig. 1. Simulated and extracted energy band diagram, electric field, and band-to-band generation rate G_{BTBT} along the source-to-channel direction at 1 nm below the surface for a double gate Si TFET by using MEDICI. (a) local model (b) non-local model. Device parameters: L_G = 60 nm; T_{ox} = 0.8 nm. The p+ source and n+ drain have a doping concentration of 1 × 10^{20} cm^{-3} with abrupt doping profiles.

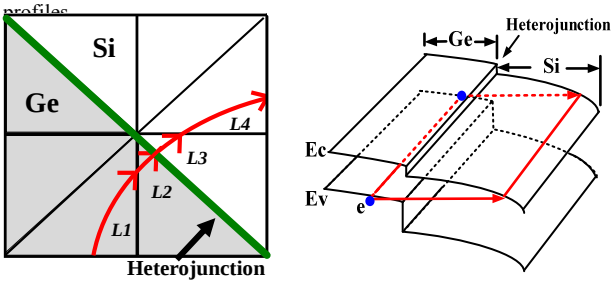


Fig. 3. (a) Schematic of single tunneling path across heterojunction. (b) *3-D* plot of energy band diagram along source-to-channel direction where electrons tunnel from valence band of Ge to the conduction band of Si at energy E. (c) Simulated *2-D* energy band diagram along source-to-channel direction in a heterostructure TFET device.

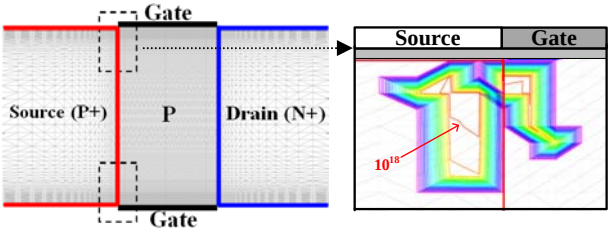


Fig. 5. (a) Mesh Structure of proposed double-gate n-channel Ge-Source Si TFET with L_G = 60 nm and T_{ox} = 0.8 nm. The p+ source and n+ drain have a doping concentration of 1 × 10^{20} cm^{-3} with abrupt doping profile at gate edge. The band-to-band tunneling mainly happens in the region enclosed with dot line near source. (b) Contour of simulated electron and hole generation rate G_{BTBT} (cm^{-3} s^{-1}) for devices as described in (a), where V_{DS} = 1 V, V_{GS} = 1.2 V. The highest G_{BTBT} (~10^{18} cm^{-3} s^{-1}) has been colored in red and the difference between two neighbor contour line is one order.

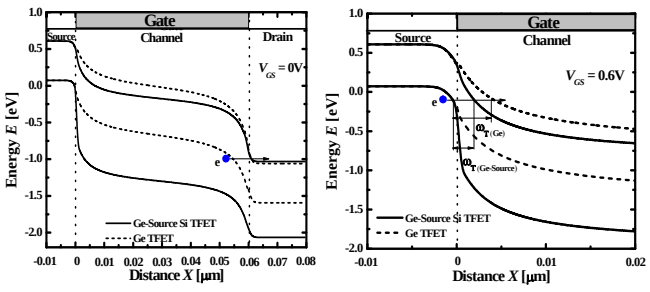


Fig. 7. Simulated energy band diagrams along the source-to-channel direction at 1 nm below the surface for Ge and Ge-source Si TFETs with V_{DS} = 1 V. (a) In the off-state (V_{GS} = 0 V), the small ω_T in Ge-TFET contributes higher I_{off}. (b) In the on state (V_{GS} = 0.6 V), the Ge-source Si TFET has narrower ω_T (~2.3 nm) compared to that of Ge TFET (~4.2 nm) which gives rise to a higher I_{on} for Ge-source Si TFET.

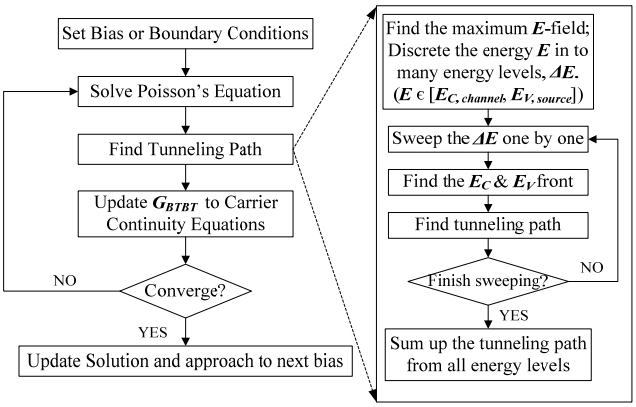
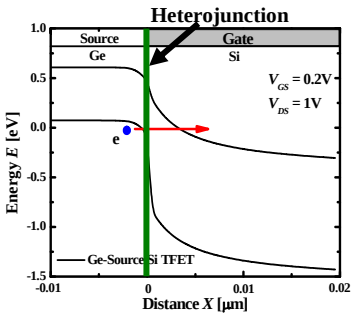


Fig. 2. Flow chart illustrating the GSS non-local algorithm of calculating BTBT current for TFET application.



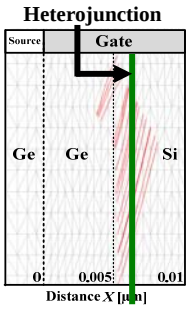


Fig. 4. Simulated and extracted tunneling path for ΔE in a heterostructure TFET.

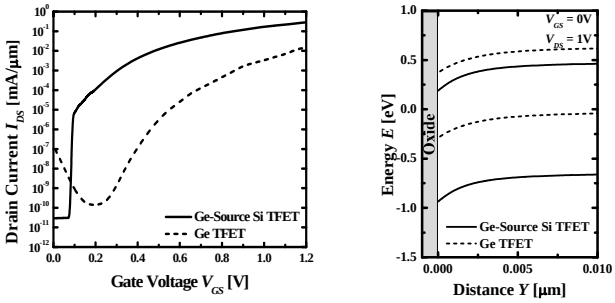


Fig. 6. (a) I_D-V_G plot for Ge-Source Si TFET and Ge TFET. Compared with Ge TFET, lower off-state current I_{off}, higher on-state current I_{on} (~0.3 mA/μm at V_{GS} = 1.2 V) , much steeper subthreshold swing S (~10 mV/decade) and lower V_T (~0.2 V) have been observed in Ge-Source Si TFET. (b) Simulated energy band diagram along gate-to-channel direction at 1 nm away from the source-gate edge.

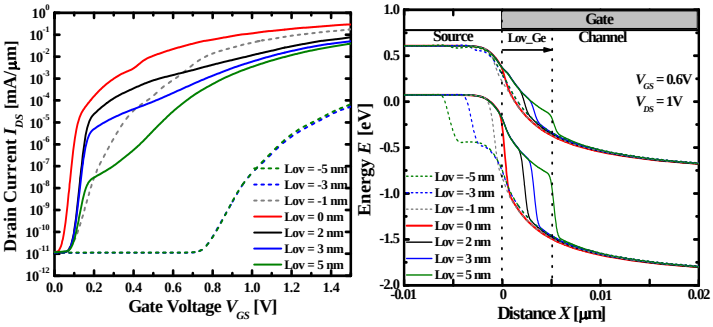


Fig. 8. (a) I_D-V_G plot for the Ge-Source Si TFET as described in Fig. 5 except that the L_{ov} varies from -5 nm to 5 nm (V_{DS} = 1 V). (b) Simulated energy band diagrams along the source-to-channel direction at 1 nm below the surface, where V_{DS} = 1 V, V_{GS} = 0.6 V.