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Anisotropic transport in epitaxial graphene transistor on vicinal SiC substrate

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1. Introduction

Remarkable electric properties of single or multiple carbon atomic sheets of graphene have been revealed in theoretical and experimental studies for several years [1]. Based on the high carrier mobility, transistor application, such as ultrafast electronics, is expected as a future nano-electronics. For a development and realization of the graphene field-effect transistors (FETs), large-area sheet of several-inch scale would be desired.

Recently, a growth process of epitaxial graphene layers is studied by using SiC decomposition at high temperatures [2]. The vicinal SiC substrate surface has self-organized periodic atomic step structures (nanofacets), which makes a difference to the growth process, and can supply large and relatively uniform epitaxial graphene layers. However, the periodic nanofacet may possibly cause an anisotropic transport in the graphene sheets, because electric conduction in the atomic sheet might be sensitive to the atomic-surface condition on the substrate. Especially, for the transistor application, the transistor properties will be changed by current flow direction.

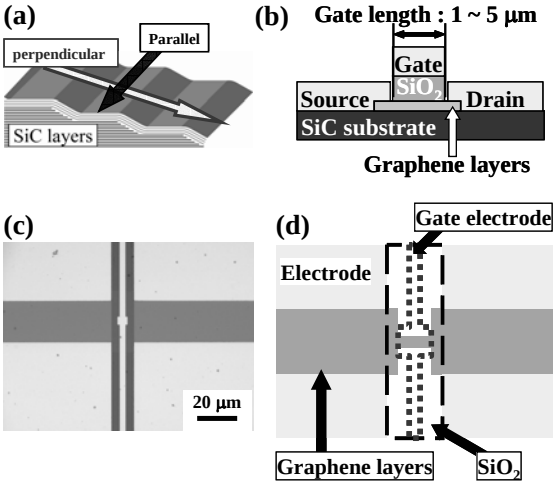

Fig. 1 (a)Schematic of vicinal SiC surface with current flow directions in step structures. (b)Cross-sectional schematic image of graphene FET. (c)Optical microscope image of the FET in four-terminal configuration. (d)Schematic image of the FET.

2. Experiment

In order to investigate this effect, graphene FETs were fabricated on vicinal SiC substrates with the channels parallel (parallel-channel FET) or perpendicular to the nanofacet (perpendicular-channel FET) (Fig. 1(a)). First, 2-3 graphene layers were grown on the Si face of vicinal 4H-SiC substrates by thermal decomposition at 1600 °C in vacuum. Cross-sectional transmission electron microscopy revealed that the epitaxial graphene layers continuously cover the nanofacets [3]. The graphene is composed of two regions: flat regions with atomic flatness and slop regions on nanofacets. The typical period of the flat and slop cycle is 30 nm. The graphene layers were patterned by dry etching with O_2 plasma. Source and drain electrodes, and a top gate structure were formed on the graphene layers (Fig. 1(b)).

3. Result and discussion

The sheet resistivity as a function of the gate voltage was measured at room temperature in parallel or perpendicular configuration (Fig. 2). The solid line is for a parallel-channel FET and the dashed is for a perpendicular-channel. The sheet resistivities of both FETs are modulated by the gate electric field and exhibited ambipolar behavior. In comparison of the two FETs, the parallel-channel FET exhibits lower sheet resistivity and larger gate-voltage modulation. Then, the parallel-channel FETs are lower sheet resistivities and higher electron mobilities than the perpendicular-channel. The measurement results indicate that the charge

transport in graphene strongly influenced by the atomic-scale step structure formed on the substrate. Based on the observed result, we could clarify the resistivity and gate-voltage response of the graphene in nanofacet regions and atomic flat regions.

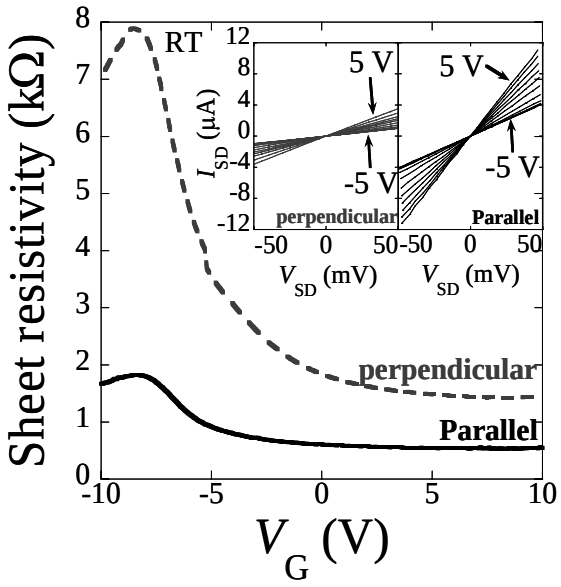

Fig.2 Sheet resistivity as a function of gate voltage observed in the transistor with 2-μm-length and 0.3-μm-width of the channel. The inset shows I_{SD} vs V_{SD}. The applied gate voltage is from -5 V to 5 V at 1 V step. The solid line is obtained in the parallel-channel FET and the dashed is in the perpendicular-channel FET.

4. Conclusions

We investigate an electrical transport property of epitaxial graphene on vicinal SiC substrate with self-organized periodic nanofacet. Anisotropic charge transport caused by current flow directions, indicating the different graphene transport properties on the terrace region and the slope were analyzed. The surface structure of SiC substrate affects the graphene growth process as well as the transistor property. This study shows that the control of self-organized nanofacet would make it possible to improve the epitaxial graphene FET performance.

Acknowledgements

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