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Characterization of Polycrystalline Silicon Thin-Film Transistors With Nickel-Titanium Oxide Gate Dielectric Coating by Sol-Gel Method

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1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention because of their various applications, such as driving circuits of active matrix liquid crystal displays (AM-LCDs) and those of active matrix organic light emitting diode displays (AM-OLEDs) [1] [2]. Solid-phase crystallization (SPC), a traditional method of fabricating poly-Si TFTs, however, could not satisfy the demands with scaling SiO_2 gate dielectric [3]. In order to overcome the issues, poly-Si TFTs with metal gate on high dielectric constant (high-κ) gate insulator have drawn a lot of attention to maintain higher gate capacitance density, lower gate-leakage current, and more carriers in channel [4]. In this paper, a novel high dielectric constant (high-κ) material of $NiTiO_3$ was used as gate dielectric of poly-Si TFTs by sol-gel spinning coating. The performances of the capacitors and the TFT devices with nickel-titanium Oxide ($NiTiO_3$) gate insulator treated at various temperatures were discussed.

2. Device Fabrication and Experimental Procedures

Fig. 1(a) illustrates the cross section of the high-κ $NiTiO_3$ capacitor. The p-type silicon substrate was subjected to RCA clean. And then, $NiTiO_3$ film was deposited by spin-coating on a 5-nm SiO_2 layer and then baked at 200°C for 5 min to remove the solvent. The $NiTiO_3$ spin process was repeated for 5 times to get a $NiTiO_3$ film thickness of around 70 nm on Si substrate. After the thermal treatment at 400°C in an N_2/O_2 ambient for 10 min, the samples were annealed at 500°C, 600°C, and 700°C for 30s in N_2 ambient by rapid thermal annealing (RTA) process. Finally, the TaN electrodes were deposited by sputter system and defined by shadow masks.

The cross section of the poly-Si TFT with TaN metal gate and $NiTiO_3$ gate dielectric is shown in Fig. 1(b). First, a 50-nm amorphous silicon was deposited on 500-nm wet oxidized Si wafers by low-pressure chemical vapor deposition (LPCVD) at 550°C. The active regions were defined after the SPC annealing at 600°C for 24 h in N_2 ambient. The source and the drain were implanted and activated at 600°C for 24 h. Then, a 70-nm $NiTiO_3$ film was deposited by the same method with the capacitor. After the deposition of a TaN film, the gate electrode was defined by plasma etching. Finally, a 400 nm passivation SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD), and the contact holes were etched by buffered oxide etch (BOE). Finally, aluminum was sputtered and defined as metal pads.

3. Results and Discussion

Fig. 2 shows the C-V characteristics of $NiTiO_3$ capacitors annealed at various temperatures, and the insert is the transmission electron microscope (TEM) image of one layer $NiTiO_3$ film of 14-nm thickness on a 5-nm SiO_2. The C-V curves of 70-nm $NiTiO_3$/5-nm SiO_2/Si substrate capacitors annealed at 500°C and 600°C present steeper slope than that at 700°C, considering a better interface between $NiTiO_3$ and Si. As RTA is at 700°C, the C-V curves degrade because of the interface-oxide growth. The dielectric constant of $NiTiO_3$ can be extracted the value of 37.9, which matches the value of the oxidized Ni/Ti films [5]. The I-V characteristics of $NiTiO_3$ gate dielectric are shown in Fig. 3. The leakage current increases with RTA temperature increasing due to the precipitation and crystallization of $NiTiO_3$ after high temperature treatment.

Figs. 3(a) to 3(c) illustrate the atomic force microscope (AFM) images of $NiTiO_3$ films annealed at 500°C, 600°C, and 700°C. Many precipitations of the film lead to significant surface roughness especially for annealing at 700°C. The root-mean-square (rms) values of the films annealed at 500°C, 600°C, and 700°C are 0.348 nm, 0.671 nm, and 2.501 nm, respectively. The serious surface roughness of $NiTiO_3$ films may cause leakage current and worse capacitance with increasing RTA temperature. Fig. 4 presents the grazing incident X-ray diffraction (GI-XRD) spectra of the $NiTiO_3$ films annealed at various temperatures. No significant signals could be found the samples annealed at 500°C and 600°C. When the sample was annealed at 700°C, the $NiTiO_3$ film was crystallized and the peak was appeared at (104), (111), (113), (116), (214), and (300). The results suggest the $NiTiO_3$ thin films annealed at 500°C remain amorphous phase.

Fig. 5 shows the transfer characteristics for the poly-Si TFTs with $NiTiO_3$ gate dielectric annealed at various temperatures. The driving current of poly-Si $NiTiO_3$ TFT at 500-°C RTA is found to be the best one compared with that at higher temperature because of better capacitor performance of 500°C RTA. Gate-induced drain leakage (GIDL) of poly-Si $NiTiO_3$ TFT at 500-°C RTA is also the best of the three. The output characteristics of poly-Si $NiTiO_3$ TFT annealed at various temperatures were inserted in Fig. 5. The driving current enhancement of the high-κ TFTs results from the high capacitance density induced higher mobility and smaller threshold voltage. As being seen, the driving current of poly-Si $NiTiO_3$ TFTs annealed at 500°C is larger than that of those annealed at 600°C and 700°C.

The threshold-voltage roll-off properties are shown in Fig. 6. The threshold voltage of the poly-Si TFTs with 70-nm TEOS gate dielectric is decreased with scaling down channel length due to the reduction of grain-boundary trap states. On the other hand, the poly-Si TFTs with $NiTiO_3$ gate dielectric demonstrate high gate capacitance density to quickly fill up the grain-boundary trap states and have better turn-on characteristics. Therefore, the threshold-voltage roll-off properties could be controlled well.

4. Conclusions

In this paper, capacitors with high-κ $NiTiO_3$ gate dielectric using sol-gel spin-coating and Poly-Si TFTs with $NiTiO_3$ gate dielectric and TaN metal gate, have been fabricated. The physical and electrical characteristics of capacitors and devices are also investigated. The samples of the spin-on $NiTiO_3$ thin film annealed at 500°C have the best performance including higher gate capacitance, lower leakage current, and higher driving current capability compared with those annealed at 600°C and 700°C. These results suggest that $NiTiO_3$ thin films annealed at 500°C remain amorphous phase.

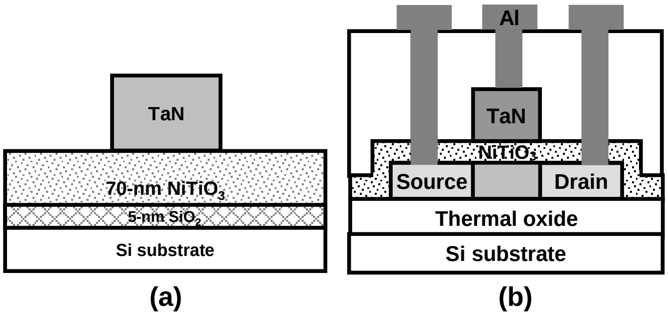

Fig. 1. The schematic cross section of (a) the high-κ $NiTiO_3$ capacitor, and (b) the poly-Si TFTs with $NiTiO_3$ gate dielectric.

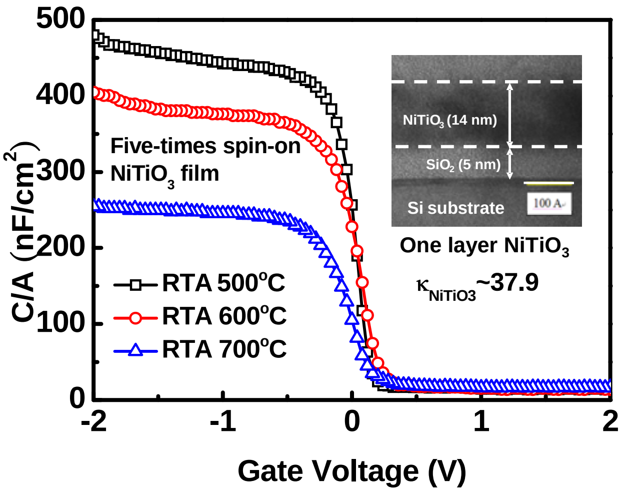

Fig. 2. The C-V curves of five-times spin-on $NiTiO_3$ films annealed at various RTA temperatures and the inset is the TEM image of one-layer $NiTiO_3$.

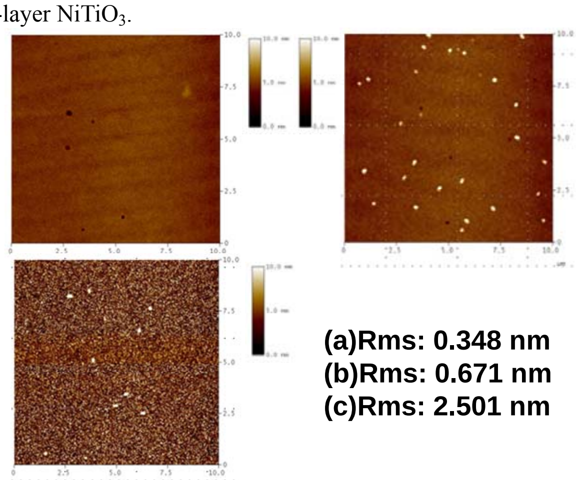

Fig. 3. The AFM images of spin-on $NiTiO_3$ annealed at (a) 500°C, (b) 600°C, and (c) 700°C.

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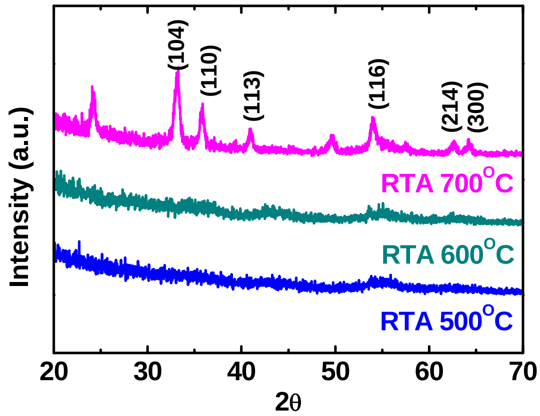

Fig. 4. GI-XRD spectra of spin-coating $NiTiO_3$ films.

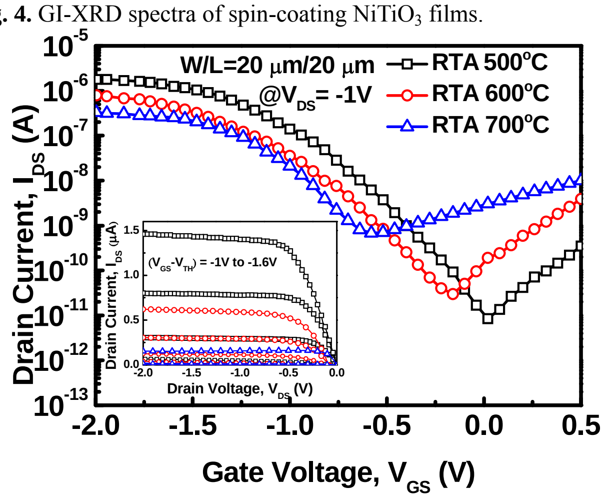

Fig. 5. The transfer characteristics of poly-Si $NiTiO_3$ TFTs with various annealing temperatures and the inset is output characteristics of poly-Si $NiTiO_3$ TFTs with various annealing temperatures

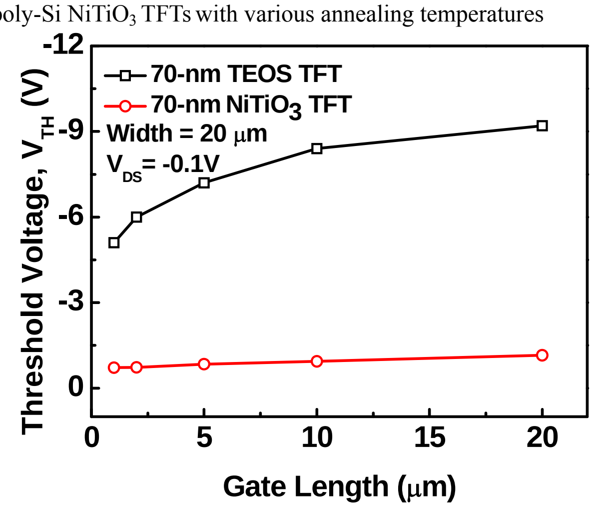

Fig. 6. Threshold-voltage roll-off properties of the poly-Si $NiTiO_3$ TFTs and the poly-Si TEOS TFTs at V_{DS} = -0.1V.