

Low-Frequency Noise in MOSFET-Based Charge-Transfer Device

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1. Introduction

The charge-transfer device consisting of two serially connected MOSFETs is very important as an element of switched capacitor circuit [1] and as a single-electron turnstile or pump [2]. Since the low-frequency noise in the MOSFET becomes increasingly conspicuous as its size is reduced, it is worthwhile to analyze the noise behavior of the charge-transfer device with small dimensions.

In this paper, current noise in the charge-transfer devices fabricated by 65-nm bulk CMOS process is reported in comparison with the ordinary noise of a MOSFET in direct-current (DC) operation. The noise in the transfer current at a low temperature is also evaluated, and is found to show anomaly.

2. Experiments

Figure 1(a) shows the planar view of the fabricated device. Two lower gates cross the Si active area between n⁺-doped source/drain regions. An upper gate made of metal covers the active area to electrically induce an inversion layer that serves as a source/drain extension. The gate length L , channel width W and gate spacing S are 60-80 nm, 100-120 nm and 160-180 nm, respectively, and the gate oxide thickness is 5 nm.

For the charge-transfer operation, as shown in Fig. 1(b), pulses with a phase delay of 180 deg are applied to the V_{lg1} and V_{lg2} to alternately turn on and off the channels. The current is measured with Agilent 4156C, and the sampled data are Fourier transformed to the noise power spectrum.

3. Results and Discussions

The charge transferred in one cycle of the pulse is expressed as [3]

$$Q = C_{\Sigma}' V_d + C_{lg1} (V_{tho1} - V_{lg1L}) + C_{lg2} (V_{lg2L} - V_{tho2})$$

where $C_{\Sigma}' = C_{lg1} + C_{ug} + C_b + C_s + C_d$, V_{lg1L} and V_{lg2L} are the lower levels of the V_{lg1} and V_{lg2} pulses, respectively, and V_{tho1} and V_{tho2} are the threshold voltages of FET1 and 2, respectively, when source/drain is not biased. Note that the noise in the form of the fluctuation in V_{tho1} and V_{tho2} leads to the fluctuation in Q , and is reflected to the noise in the transfer current $I_d = Qf$, where f is the pulse frequency.

Figure 2 shows the charge transfer (I_d - V_{ds}) characteristics at 295 K for various pulse frequencies. Since the slope of the curve (i.e. conductance) is proportional to the frequency, C_{Σ}' can be calculated to be 4.0 aF.

At V_{ds} of 0.1 V, current noise spectra are evaluated at various current levels (i.e. various frequencies) as shown in Fig. 3(a). The current noise spectra for DC operation are

also obtained with the same device by applying high voltage (2 V) to one lower gate and adjusting the other to attain the similar current levels [Fig. 3(b)]. The spectra for charge-transfer operation show larger slopes, and may be characterized as $1/f$. Those for DC operation show gentler slopes, and may be regarded as the low-frequency part of Lorentzian mixed with $1/f$.

The power spectral densities at 1 Hz, obtained by extrapolating the fitted lines, are plotted with respect to the average current. It can be seen that an order of magnitude smaller current noise is attained in the charge-transfer operation. In association with the cycled-gate experiment [4], this reduction can be attributed to the reduced capture time to the interface traps possibly caused by the high concentration of inversion or accumulation charges.

Figure 5 shows the charge-transfer characteristics at low temperature, where current quantization can be expected as a result of Coulomb blockade [2]. However, the current plateaus do not perfectly match the multiple of eI and large noises are found to be superimposed. In order to simply characterize the noises, plateau areas are chosen, straight lines are drawn by least-square method, the square of the deviation from the straight lines are averaged to obtain noise power, plotted as a function of current in Fig. 6. Two orders of magnitude larger noise is seen at 20 K, which might be caused by the prolonged emission and capture times.

3. Conclusions

Current noise in the MOSFET-based charge-transfer device is evaluated. It is found that, at 295 K, the noise is an order of magnitude smaller than that in DC operation presumably due to the reduced capture time to the interface traps. At 20 K, on the contrary, two orders of magnitude larger noise is found in the transfer current, which might be caused by the prolonged emission and capture times. The reduction of the interface traps is especially significant for the single-electron transfer at low temperatures.

Acknowledgements

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References

- [1] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, chap. 7 and 12, McGraw-Hill, 2001.
- [2] A. Fujiwara, et al., Appl. Phys. Lett. **84** (2004) 1323.
- [3] H. Inokawa, et al., Ext. Abstracts of SSDM (2007) 874.
- [4] B. Dierickx and Simoen, J. Appl. Phys. **71** (1992) 2028.

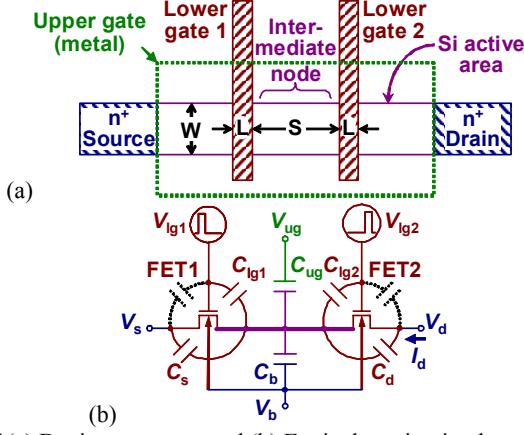


Fig. 1(a) Device structure, and (b) Equivalent circuit when operating as a charge-transfer device

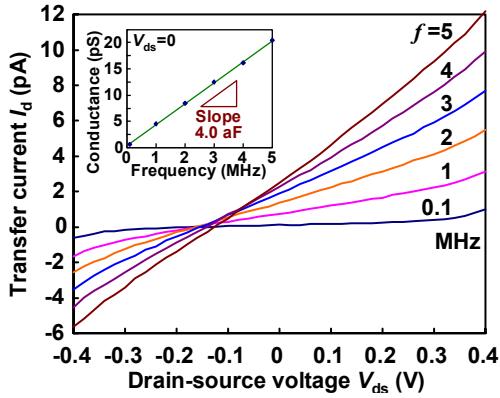


Fig. 2 Charge-transfer (I_d - V_{ds}) characteristics at 295 K. $L=70$ nm, $W=110$ nm, $S=170$ nm.

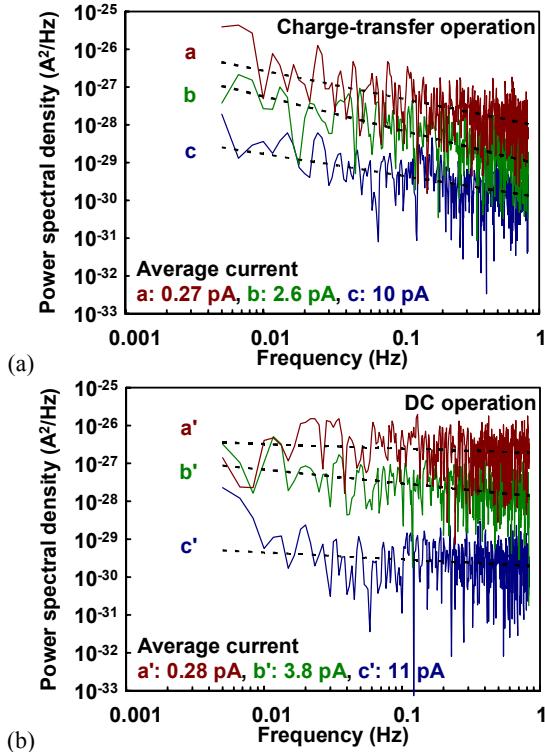


Fig. 3 Noise power spectra in (a) charge-transfer, and (b) DC operations at 295 K. $L=70$ nm, $W=110$ nm, $S=170$ nm.

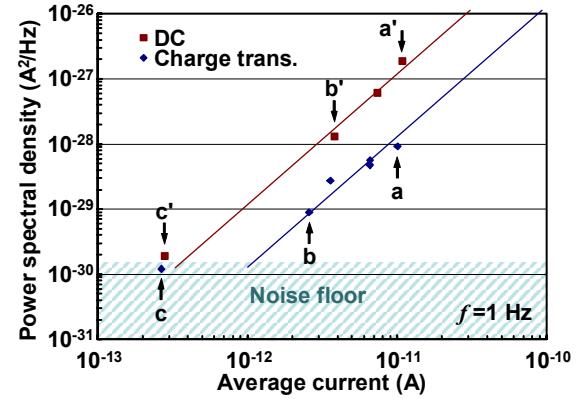


Fig. 4 Noise power density vs. current for DC and charge-transfer operations at 295 K. $L=70$ nm, $W=110$ nm, $S=170$ nm.

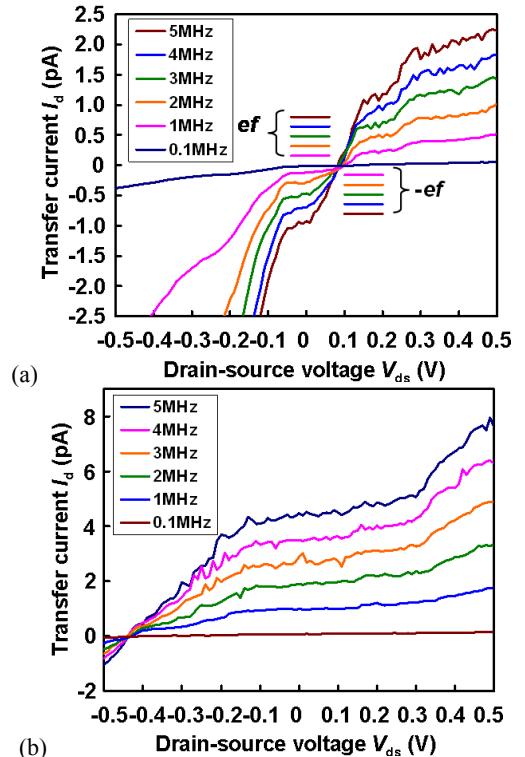


Fig. 5 Charge-transfer (I_d - V_{ds}) characteristics at 20 K. (a) $L=60$ nm, $W=100$ nm, $S=160$ nm, (b) $L=80$ nm, $W=120$ nm, $S=180$ nm.

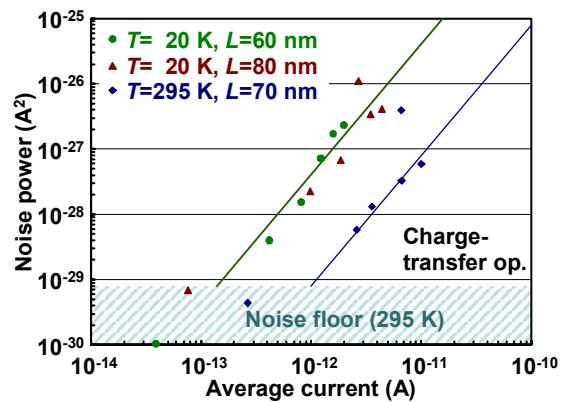


Fig. 6 Total noise power vs. current for charge-transfer operation at 20 and 295 K. Excess noise is observed at low temperature.