Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp597-598

Capacitances in Tunneling Field-Effect Transistors

Yue Yang, Xin Tong, Li-Tao Yang, Peng-Fei Guo, Lu Fan,
Ganesh S. Samudra, Yee-Chia Yeo*

Dept. of Electrical & Computer Engineering, National University of Singapore (NUS), 117576 Singapore.
* Phone: +65 6516-2298, Fax: +65 6779-1103, E-mail: yeo@ieee.org

1. Introduction

Scaling of conventional CMOS device dimension and supply voltage V_{DD} faces fundamental limitation associated with the non-scalability of the subthreshold swing *S*, which has a lower limit of 60 mV/decade at room temperature. Tunneling field-effect transistor (TFET), which exploits the gate-controlled band-to-band tunneling (BTBT) phenomenon to achieve steep *S*, is a promising device option to overcome this limitation [Fig. 1(a)-(b)]. TFETs can achieve a high I_{on}/I_{off} ratio at significantly reduced V_{DD} and power consumption, and have attracted a lot of research interest, especially in device simulation and fabrication [1]-[9]. It should be noted that capacitance is a crucial determinant of switching speed in integrated circuits, and a detailed understanding of TFET capacitances will be very important. There is little or no investigation on TFET capacitance components and their distribution within the device.

In this work, we report the first analysis of capacitance components in a planar TFET device. The dependence of capacitances on terminal voltages and device geometry are investigated using a physics-based TCAD simulator [10]. Key differences with MOSFET capacitance distribution are highlighted. A compact TFET capacitance model comprising parasitic capacitances and inversion capacitances is built. The impact of drain dopant profile engineering on TFET parasitic capacitances is also studied.

2. MOSFET gate capacitance vs TFET gate capacitance

In the on-state, the inversion charge distribution in a TFET is significantly different from that of a MOSFET. At low V_{ds}, both the source and drain of a MOSFET are connected to the inversion layer [Fig. 1(a)], and the partitioning of C_{gg} between the source and drain terminals is approximately symmetric. For a TFET, the drain is connected to the inversion layer, and the inversion carrier density is dependent on the position of the Fermi level in the drain. For large V_{ds}, the TFET inversion layer pinches off at the source side [9], not the drain side. The distribution of capacitance components within the TFET device is fundamentally different from the MOSFET. Even at V_{ds} = 0 V, C_{gd} and C_{gs} are asymmetrically distributed in a TFET, as shown in Fig. 1(c), where C_{gd} dominates the total gate capacitance C_{gg}.

At $V_d = V_s$ = 0 V and V_g = 1 V, the simulated inversion carrier concentration, n^+ poly-Si depletion charge, and energy band diagram are shown in Fig. 2. By computing the change in gate charge with respect to a small change in a terminal voltage, a capacitance component at a bias point may be calculated, e.g. $C_{gd} = dQ_g/dV_d$.

3. TFET gate capacitance components and modeling

Geometry-based TFET capacitance analysis is performed and various capacitance components are identified accordingly (Fig. 3). In the off-state, both C_{gd} and C_{gs} in a TFET comprises parasitic capacitance components; while in the on-state, C_{gd} is dominated by the inversion capacitance $C_{gd,inv}$. A complete set of C_{gd} and C_{gs} at various V_{gs} is extracted from our simulation data (Fig. 4).

As mentioned, source-side inversion layer pinch-off occurs in the saturation regime of the TFET I_d-V_d characteristics. We therefore observe that V_{gd} empirically controls the inversion layer density and its length or the extent of its reach towards the source. The strong dependence of C_{gd} on V_{gd} is clearly demonstrated in Fig. 4. For positive V_{gd}, C_{gd} is mainly contributed by the inversion capacitance $C_{gd,inv}$. With increasing V_{gd}, the length of the inversion layer increases, contributing to an increase in $C_{gd,inv}$. C_{gs} is smaller and less strongly dependent on V_{gd}. C_{gs} falls as V_{gd} rises due to the screening effect of the inner fringing capacitance when channel is inverted.

A compact TFET *C-V* model is then built based on the parasitic capacitance components (C_{dif}, C_{dov}, C_{dof}, C_{sif}, and C_{sof}) and inversion capacitance ($C_{gd,inv}$). The equivalent circuit is showing these components in Fig. 3 (left), and equations used in the compact model are detailed in Fig. 3 (right). Similar to MOSFET *C-V* modeling, the capacitances components that are gate length independent are defined as extrinsic capacitances, and usually comprise parasitic components. Intrinsic capacitance components are those that scale proportionately to the gate length, e.g. $C_{gd,inv}$ (Fig. 5). We define the V_{fb} as the transition point from extrinsic to intrinsic, which is a key parameter used in C_{gd} modeling. The compact *C-V* model achieves reasonably agreement with TCAD simulation at various V_g and V_{ds} biases (Fig. 6). All the components in the model are physical, and the model describes the biases dependence of TFET *C-V* characteristics very well.

4. TFET gate capacitance comparison and parasitic capacitance reduction by drain engineering

Devices simulated so far employ n^+ poly-Si gate with gate depletion effects fully accounted for. The use of metal gate in a TFET leads to a comparatively larger C_{gg} due to the elimination of gate depletion effects under inversion bias. This is shown in Fig. 7. Metal gate adoption increases the intrinsic TFET capacitance.

To improve transient performance in circuits employing TFET, the parasitic capacitance components need to be reduced. Two TFET parasitic capacitance reduction schemes are proposed here, and both are related to drain engineering (Fig. 8). First, making the drain doping more abrupt helps to suppress parasitic capacitance due to reduction of the drain overlap capacitance C_{dov} under the gate (Fig. 7 and 8), which is around 28% reduction (Table. I). Second, moving the drain region further out, i.e. introduce an offset as shown in Fig. 8, also reduces gate parasitic capacitance. This is due to the elimination of C_{dov} and reduction of C_{dof}. The reduction of parasitic capacitance can reach 52-53% (Table. I) at the cost of an increased layout space.

5. Conclusions

We performed a study of capacitances in a TFET, and obtained the partitioning of the gate capacitance into C_{gd} and C_{gs} from 2D TCAD simulation at various biases. A compact model for TFET capacitances was built, which accounts for parasitic and inversion capacitance components. Good agreement between compact model and TCAD simulation was observed. We also examined methods of drain engineering, e.g. doping abruptness and introduce of drain offset, for reduction of drain parasitic capacitance.

Acknowledgement We acknowledge research grant (Award number NRF-RF2008-09) from the National Research Foundation (NRF).

References

[1] Th. Nirschl *et al.*, *IEDM 2004*, pp. 195.
[2] K. K. Bhuwalka *et al.*, *IEEE Trans. Elect. Dev.* 51, pp. 279, 2004
[3] W. Y. Choi *et al.*, *JJAP*, pp. 2622, 2007.
[4] E.-H. Toh *et al.*, *APL* 91, pp. 263507, 2007.
[5] E.-H. Toh *et al.*, *JJAP* 47, pp. 2593, 2008.
[6] T. Krishnamohan *et al.*, *IEDM 2008*, pp. 947.
[7] F. Mayer *et al.*, *IEDM 2008*, pp. 163.
[8] A. Bowonder *et al.*, *IWJT 2008*, pp. 93.
[9] C. Shen *et al.*, *IEEE EDL* 29, pp. 1252, 2008.
[10] C. Shen *et al.*, *VLSI-TSA 2009*, pp. 119.
[11] F. Preqaldiny *et al.*, *Solid-State Electronics* 46, pp. 2191, 2002.
[12] BSIM3 v3.2 User Menu.
[13] C. Kshirsaqar *et al.*, *DAC 45th ACM/IEEE*, 2008

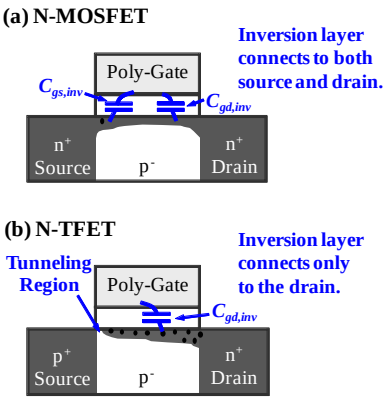

Fig. 1. Key difference in inversion charge distribution in (a) an N-MOSFET and (b) an N-TFET, both with n^+ poly-Si gate. (c) C_{gs} and C_{gd} plot showing the asymmetric partitioning of gate capacitance in an N-TFET at V_{ds} = 0 V.

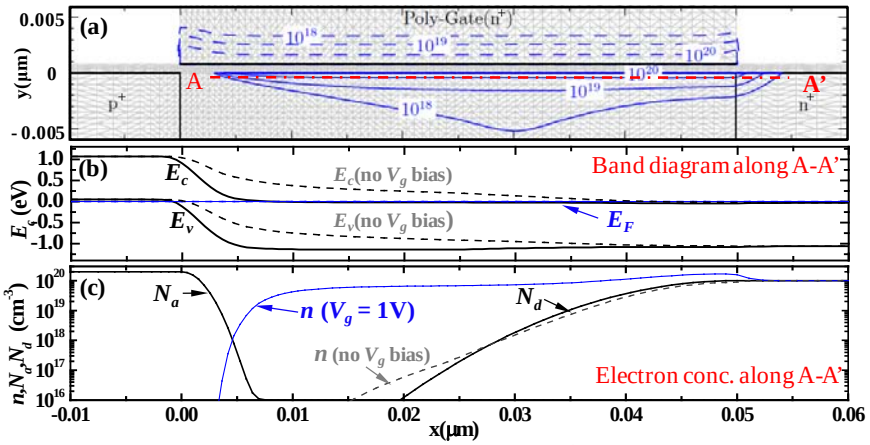

Fig. 2. (a) Contour plot showing inversion carrier concentration n (in cm^{-3}) in the substrate (solid) and depletion charge (N_d-n) (cm^{-3}) in the gate (dash) when V_g = 1 V and V_d = V_s = 0 V. (b) Energy band diagram and (c) profile of N_a, N_d and n underneath the gate (along A-A') at V_g = 1 V (solid line) and 0 V (dashed line).

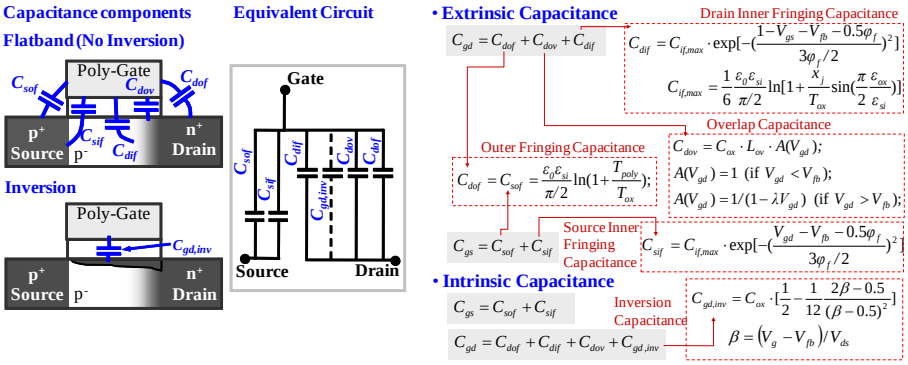

Fig. 3. TFET capacitance components and equivalent circuit (left). C_{sof} and C_{dof} are the outer fringing capacitances at the source and drain, respectively. C_{sif} and C_{dif} are the inner fringing capacitances at the source and drain respectively. C_{dov} is drain overlap capacitance. Under inversion bias, the inversion capacitance, $C_{gd,inv}$, is present. Equations are quoted or derived from [11]-[13].

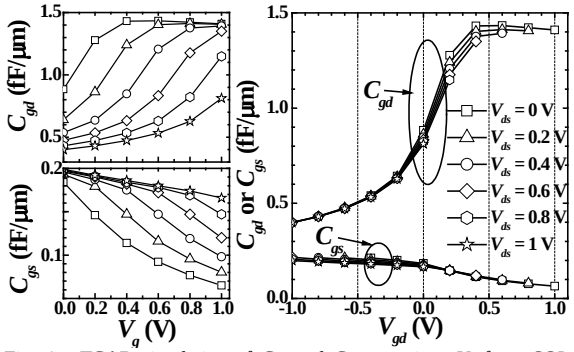

Fig. 4. TCAD simulation of C_{gd} and C_{gs} at various V_g for a SOI TFET with L_g = 50 nm, EOT = 0.8 nm, abrupt source profile (N_a = 2×10^{20} cm^{-3}) and gradual drain profile (N_d = 10^{20} cm^{-3}). V_s = 0. C_{gd} has strong dependence on V_{gd} and C_{gs} has some dependence on V_{gd}.

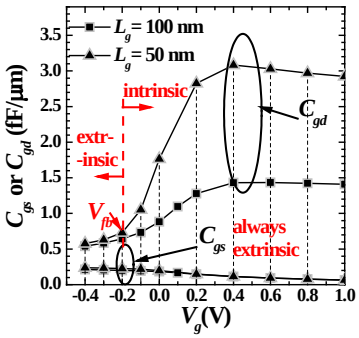

Fig. 5. Definition of intrinsic and extrinsic capacitance of TFET. The transition point defined as V_{fb}.

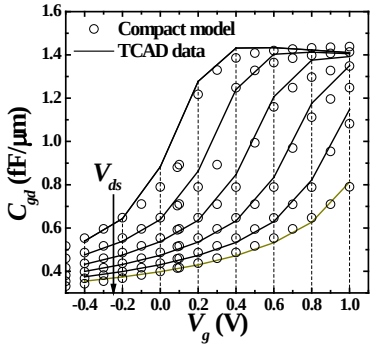

Fig. 6. Comparison between compact modeling (open circles) with TCAD simulation data (solid lines). The C_{gd} curves are obtained at various V_{ds} bias from 0~1 V in steps of 0.2 V.

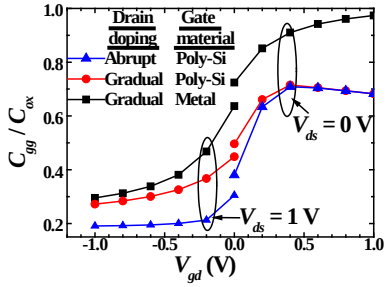

Fig. 7. Difference in C_{gg}/C_{ox} for various device design combinations: Metal or Poly- Gate; Gradual or Abrupt Drain Doping.

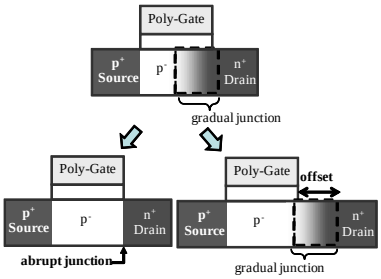

Fig. 8. TFET drain parasitic capacitance can be reduced by making the drain doping more abrupt or by using an offset drain.

Table I. List of capacitances improvement schemes obtained by TCAD simulation

	Drain Design		Minimum C_{gg}/C_{ox} (extrinsic)	Reduction % of minimum C_{gg}/C_{ox}	Maximum C_{gg}/C_{ox} (intrinsic)
	Abrupt	With offset			
PolySi Gate			0.264	0	0.683
	√		0.191	27.7%	0.689
		√	0.126	52.3%	0.689
	√	√	0.120	53.0%	0.689
Metal Gate			0.283	0	0.968
	√		0.203	28.3%	0.967
		√	0.135	52.3%	0.966
	√	√	0.128	54.7%	0.966