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Nonvolatile memory thin film transistors using triple polymeric dielectric layers

Ying-Chih Chen[1,2], Chun-Yuan Huang[3], Chiao-Yang Cheng[1,2], Hsin-Chieh Yu[1,2], Yan-Kuin Su[1,2,*], Tai- Hsiang Chang[1,2]

[1] Institute of Microelectronics, National Cheng Kung University, Tainan 70101, Taiwan
[2] Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan 70101, Taiwan
[3] Department of Applied Science, National Taitung University, Taitung, 950, Taiwan
*Phone: +886-6-2757575-62382 E-mail: yksu@mail.ncku.edu.tw

1. Introduction

In recent years, due to the quick development of the flexible electronic applications such as the smart tag, radio frequency identification tag, e-signage, flexible sensor, and flexible display, the organic-based memories become an indispensable device. Basically, the memory devices can be divided into three primary categories according to the device architecture: capacitor-, transistor- and resistor-type memories[1]. Among them, the transistor-type memories showed the most promising capabilities for their high flexibility. The memory behavior of transistor-type devices typically comes from the properties of gate dielectric materials. A polymer ferroelectric thin film, such as poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) [2], and poly-m-xylylene adipamide [3] has been extensively used as the gate dielectric to accumulate channel charge by the electric dipoles and electric polarization effect. A charge electret material with the charge-storage or slow polarization capability, such as polyvinyl alcohol (PVA) [4] is also suitable as the gate dielectric for memory applications. Although novel dielectric materials are continuously discovered and reported, most of the devices are with single dielectric layer, and few attempts have been made on inorganic/organic double gate insulator [4]. In this letter, we fabricated and characterized pentacene-based OTFTs with triple polymer layers (poly(2-hydroxyethyl methacrylate) (PHEMA)/poly(methyl methacrylate) (PMMA)/PHEMA). After we optimized the device structure, large memory window (hysteresis characteristic) for drain-source current with variation of gate voltage (V_{GS}) was observed.

2. Experimental Details

The device design and fabrication process are explained as follows. An indium tin oxide (ITO, 10 Ω/□) thin film coating on the glass was used as the gate electrode of OTFTs. Solutions of 5 wt% PMMA (molecular weight = 996,000) in toluene and 4 wt% PHEMA (molecular weight = 1,000,000) in methanol were prepared for depositing blocking and charge-storage layer, respectively. After cleaning the patterned ITO glass, three different architecture of gate dielectric, PHEMA/PMMA/PHEMA, PHEMA/PMMA and PMMA/PHEMA, were separately formed on the ITO thin films by spin-coating and heating techniques. The thicknesses of PMMA and PHEMA film were measured to be about 200 and 350 nm, respectively. A

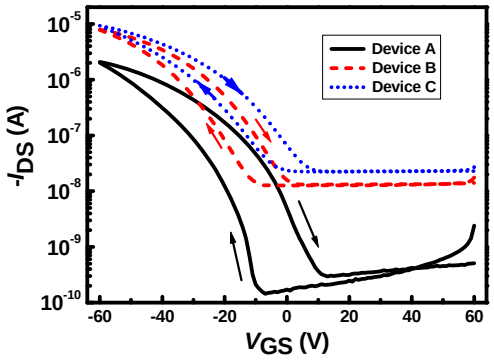

Fig. 1 Transfer characteristics of OTFTs at fixed V_{DS} of -40 V.

60-nm-thick pentacene as the channel layer was then deposited on these dielectric layers through the shadow mask by thermal evaporation under a vacuum level of 1×10^{-6} Torr, followed by the thermal evaporation of a 150-nm-thick gold thin film to define the source and drain electrodes. The channel length and width of the devices were 100 and 500 μm, respectively. Finally, the OTFTs with triple, PHEMA/PMMA, and PMMA/PHEMA dielectric layers were then marked as Devices A, B, and C, respectively.

3. Results and Discussion

The transfer characteristics were measured with forward and reverse gate voltage (V_{GS}) sweeping between 60 and -60 V at a sweep rate of 5 V/s at a fixed drain voltage (V_{DS}) of -40 V, as shown in Fig. 1. These devices exhibit the behavior of *p*-channel field-effect transistors, as well as the noticeable clockwise hysteresis loops. The field-effect mobility (μ) for Devices A, B, and C can be calculated by using current voltage equation of field-effect transistors[10], which is 0.17, 0.66 and 0.7 cm^2/V-s, respectively. Most importantly, Device A exhibits a memory current on/off ratio ($I_{on/off}$) 10 times larger than that of the other two devices and a larger threshold voltage shift ($\triangle V_T$). Here $I_{on/off}$ is defined as the ratio of the maximum to minimum drain-source current (I_{DS}) at the same gate bias during a single sweep.

To realize the memory mechanism for these devices, the characteristics of the write-read-erase-read cycles were repeatedly measured and the results are shown in Fig. 2. The write operation was achieved by a negative voltage pulse (-60 V), while the erase operation was implemented

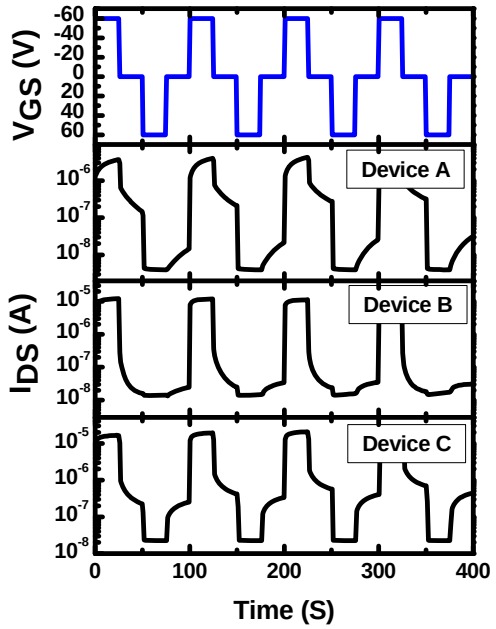

Fig. 2 Retention measurements of the devices. Filled triangle/circle and opened triangle/circle represent the LRS/HRS of PHEMA-/PMMA-devices, respectively.

by a positive voltage pulse with the amplitude of +60 V. A zero gate voltage was used to read the current (the state) of the Device after the write or erase operation. During the measurement, the drain-source voltage (V_{DS}) was fixed at -40V. A larger probe current ratio after writing and erasing is found for Device A, which indicates that the charge relaxation process for Device A is slower than that for the other devices. From previous reports about OTFTs using hydroxyl-rich gate dielectric, the hysteresis and memory behavior in OTFTs are normally attributed to four mechanisms: (1) slow polarization effect in the bulk gate dielectric [5], (2) charge trapping effect by channel/dielectric interface [6], (3) charge storage in the dielectric[7], and (4) electrical dipole effect from the polymer multilayers [8]. In this report, we propose that the memory effect is due to the locally trapped charges that induce memory window. When the large negative gate voltage is applied, the charges are trapped by -OH groups in triple dielectrics. Afterwards, the accumulation of charges may give rise to the generation of the built-in electric field in dielectric layers. The electric field points toward the opposite direction of the applied field. The locally trapped charges cannot instantly escape unless a large positive voltage (+60V, in our case) is applied, therefore, the write state will be continuously presented, until the charges are de-trapped and the device become in erase state.

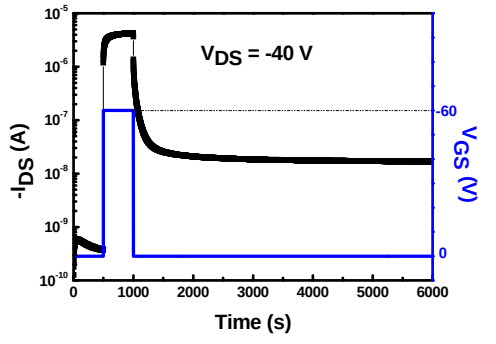

Fig. 3 Retention property of Device A at the read voltage of -40 V after writing.

To estimate the retention time of Device A, the time-resolved characteristics were also measured, as shown in Fig. 3. A reading voltage was firstly applied to measure the current of the device in the off-state. After writing voltage of V_{GS} = -60 V has been applied to the device for 500 s, the same reading voltage for monitoring the on-state current is applied every 1 s. When the monitor time is prolonged, it can be observed that two states are clearly distinguished. The time domain measurement data is fitted by using third order exponential decay plus a stretched exponential equation [6]. The trend of drain current decay at 3500 s $\leq t \leq$ 5000 s is well described by a stretched exponential in curve flitting. This period exhibits the third order exponential decay. The best-fit values of relaxation time (τ) and power (β) are 6.48×10^4 s and 0.4, respectively. This result indicates that the memory effect in device A would be prolonged for hours.

4. Conclusions

In conclusion, the nonvolatile memory OTFTs with triple dielectric layers have been demonstrated. In our device configuration, the memory effect originates from the charges stored in the interfaces between the dielectric layers and in the -OH groups inside the polymer dielectrics. The transistors have a switchable channel current and long retention time.

Acknowledgements

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