

Organic CMOS Logic Papers with In-Field User Customizability

Tsuyoshi Sekitani¹, Koichi Ishida², Naoki Masunaga², Ryo Takahashi², Shigeki Shino³, Ute Zschieschang⁴, Hagen Klauk⁴, Makoto Takamiya², Takayasu Sakurai⁵, and Takao Someya^{1,6}

¹Department of Electrical and Electronic Engineering, The University of Tokyo,
7-3-1, Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

Phone: +81-3-5841-0413 E-mail: sekitani@ee.t.u-tokyo.ac.jp

²VLSI Design and Education Center and Institute of Industrial Science, The University of Tokyo
4-6-1 Komaba, Meguro-ku, Tokyo, 153-8505, Japan

³Mitsubishi Paper Mills Ltd., Tokyo, Japan

⁴Max Planck Institute for Solid State Research, Heisenbergstr. 1, Stuttgart, 70569 Germany

⁵Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan

⁶Institute for Nano Quantum Information Electronics (INQIE), The University of Tokyo,
4-6-1 Komaba, Meguro-ku, Tokyo 153-8505 Japan

1. Introduction

On-demand user customizability of electronic logic circuits and active devices at familiar room is one of the most attracting features for next generation's electronic applications; however, until now there have been no reports, thus far. For realizing in-field user customizable electronic devices, there are two technical challenges. One is the development of electrical conductive inks that do not require any sintering processes including high temperatures and organic solvents, and can be patterned using at-home inkjet printers. Second is the integration of active components such as transistors and diodes, and passive components such as resistance, inductance, capacitances including electrical wirings.

In this work, we have demonstrated the manufacturing of user-customized logic paper—paper in which organic complementary (CMOS) logic cells are embedded (Figure 1). The logic paper provides on-demand in-field customizability to the users by making use of commercially available inkjet printing at residences. For interconnection among the logic cells, we adopted a newly developed material technology with sintering-free conductive Ag nanoparticle ink at room temperature, which can be patterned using at-home inkjet printer [1]. Organic CMOS inverters customized by this technology can operate within 2 V and signal-gain is achieved to more than 30. Furthermore, stage delay of customized organic CMOS ring oscillators is 0.12 s, indicating excellent feasibility of the logic paper.

2. Experimental results and discussions

An organic CMOS logic paper comprises an array of vias and organic CMOS based logic cells (Figure 1). Organic CMOS comprising p-type pentacene transistor (TFT) and n-type hexadecafluorocopperphthalocyanine ($F_{16}CuPc$) TFT are prefabricated and embedded in papers, and in-field customizability is provided by the at-home printed interconnects using a sintering-free Ag nanoparticle ink.

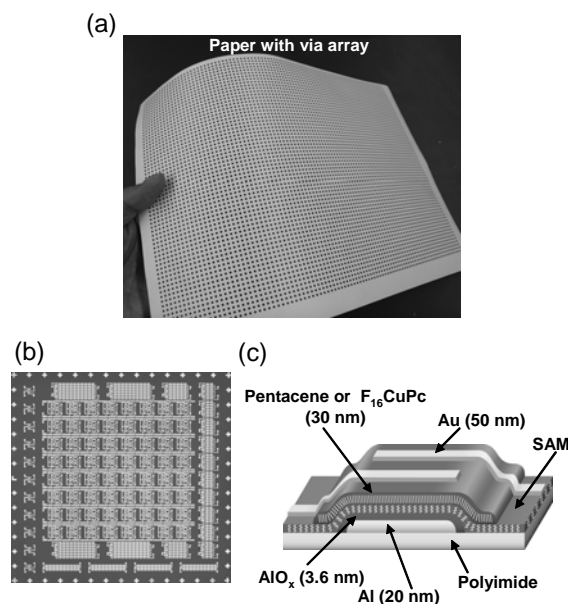


Figure 1: (a) Organic CMOS logic paper. (b) A picture of organic CMOS cell array on a polyimide film. The sheet size is 73 mm x 73 mm. (c) A cross-sectional illustration of organic TFTs

A cross-sectional illustration of the TFT can be seen in Figure 1 (c). P-type pentacene and n-type $F_{16}CuPc$ employ vacuum evaporated aluminum gate electrodes patterned by shadow masking and a gate dielectric based on a combination of a thin layer of aluminum oxide (3.6 nm thick) and a molecular self assembled monolayer (SAM) of n octadecylphosphonic acid (2.1 nm thick) [2]. The aluminum oxide film results from a brief oxygen plasma treatment required to create a sufficient density of hydroxyl groups for molecular adsorption, and the SAM is prepared from a 2 propanol solution at room temperature. The gate dielectric capacitance is $0.7 \mu F/cm^2$, so the TFTs operate with voltages between 2 and 3 V. 30 nm thick films of pentacene and $F_{16}CuPc$ are deposited in vacuum and patterned by shadow masking to provide the semiconductor films for the

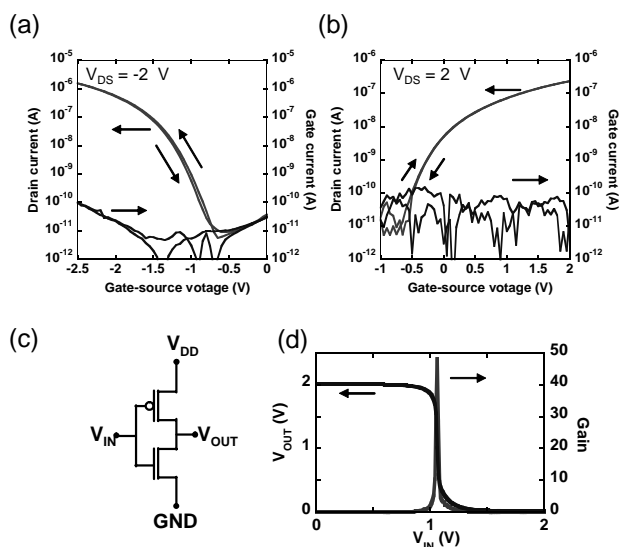


Figure 2: (a) and (b) transistor characteristics of p-type pentacene and n-type $F_{16}CuPc$ TFTs. (c) and (d) A circuit diagram and invert characteristics of an organic CMOS inverter.

p-channel and n-channel TFTs, respectively.

The DC electrical characteristics of the TFTs were measured in air using a semiconductor parameter analyzer (Agilent 4156C). Figure 2(a) show the current voltage characteristics of a p-channel pentacene TFT with a channel length of 50 μm and a channel width of 500 μm . Owing to the large capacitance of the thin gate dielectric (0.7 $\mu F/cm^2$), the TFTs show excellent linear and saturation characteristics for gate source and drain source voltages of -2 V. Despite the small thickness of the room temperature gate dielectric, the off state current at $V_{GS} = 0$ V is less than 10 pA, and the on/off current ratio is more than 10^5 . The maximum gate current at $V_{GS} = -2.5$ V is only about 100 pA. A field-effect mobility of pentacene is more than 0.3 cm^2/Vs . The transfer characteristics of an n-channel $F_{16}CuPc$ TFT are shown in Fig 2. It has a carrier mobility of 0.02 cm^2/Vs and an on/off current ratio of greater than 10^4 .

Using p-channel pentacene TFTs and n-channel $F_{16}CuPc$ TFTs with patterned Al gates, SAM based gate dielectric on a plastic substrate, we have also prepared organic complementary (CMOS) inverters. A circuit diagram and the electrical transfer characteristics of the inverter are shown in Figs. 2 (c) and (d). The pentacene TFT has a channel length of 200 μm , the $F_{16}CuPc$ TFTs has a channel length of 20 μm , and both TFTs have a channel width of 500 μm . The difference in channel length is necessary to achieve similar drain currents for both TFTs despite the significant difference in carrier mobility (0.1 cm^2/Vs for the pentacene TFT, 0.02 cm^2/Vs for the $F_{16}CuPc$ TFT). The inverter operates with supply voltages between 1.5 and 2 V and with a small signal gain greater than 45. From a circuit design perspective, complementary circuits have several advantages over circuits based on a single carrier type, including greater noise margin, lower power consumption, and faster switching speed.

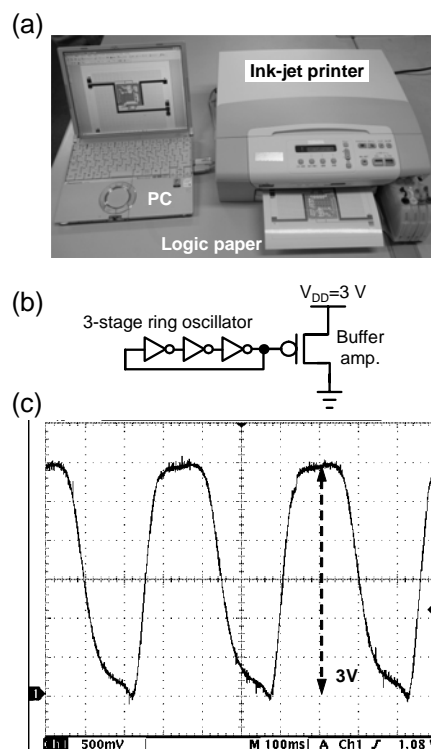


Figure 3: (a) A picture of experimental setup. (b) A picture and circuit diagram of 3-stage ring oscillator and buffer amplifier comprising organic CMOS inverters. (c) Output from the ring oscillator.

For the logic cells interconnection using inkjet printing, we adopted a newly developed conductive Ag nanoparticle ink, which can be sintered at room temperature and exhibited the sheet resistance less than 0.2 $\Omega/square$. Although the design rule of the printed interconnects strongly depends on inkjet printers, it is typically 100 μm .

Organic CMOS cells are interconnected by printed Ag nanoparticle ink at room temperature to form organic CMOS inverters and ring oscillators, which exhibit excellent electrical characteristics (Figure 3), demonstrating excellent feasibility of this technology. The organic CMOS logic paper can be utilized in a wide range of printable electronics products, including flexible displays, electronic papers, and solar cells; and especially, can also be used in education.

Acknowledgements

This study was partially supported by JST/CREST, the Grant in Aid for Scientific Research (KAKENHI; WAKATE S), NEDO, and the Special Coordination Funds for Promoting and Technology. We also thank Athene Co., Ltd for manufacturing very fine shadow masks.

References

- [1] Ishida, et al., 2010 IEEE The International Solid-State Circuits Conference.
- [2] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, Nature 445 (2007) 745-748.