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Bias-temperature-instability and thermal anneal effects of organic thin-film transistors

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1. Introduction

Organic thin film transistors (OTFTs) have been subjected energetic researches and marked with dramatic progress on the materials optimization, device fabrication, and device performance. However, organic thin film material itself is very sensitive to environmental factors such as temperature, humidity, and storage ambience, and particularly OTFTs are implemented in solution-based processes, in which inevitable residual water would be a major concern. Consequently it remains to be verified the reliability and thermal stability of OTFTs for future practical application such as flexible large-area displays, sensors, power transmission devices, and wireless identification tags.

Extensive attempts [1-4] have been made to investigate the physical origin of OTFTs electrical instability under applied bias, temperature, and time stresses, based on various organic semiconductors, polymer dielectrics, and even inorganic insulator (SiO_2). However, the instability mechanisms have been diversified since the bias-temperature stress effects are highly dependent on the processing parameters and materials. The detailed mechanisms responsible for the threshold voltage (V_{th}) instability are illusive and the major acceleration factors and models for OTFTs long-term reliability are to be determined. In this paper, bias-temperature stress effects of P3HT OTFTs with polyvinyl-phenol (PVP) gate insulator are systematically investigated in terms of V_{th}, subthreshold slope (*SS*), on-state drive current (I_{on}) and off-state leakage current (I_{off}). We attempt to provide additional insight concerning OTFT's bias-temperature instability and propose possible manner for instability recovery.

2. Experimental and Results

The fabrication of top-gate (TG) OTFTs began with a polyethylene naphthalate (PEN) substrate, which has an inkjet-printed P3HT as a semiconductor, a 510 nm-thick polyvinyl-phenol (PVP) as a gate insulator layer, and a 40 nm-thick gold as a TG electrode. The channel width (W) and length were defined as 200 μm and 20 μm, respectively. The corresponding key process flow of OTFTs is described in Fig 1. For temperature-dependent bias-stress current-voltage (*I-V*) characterization, devices were loaded into a vacuum-sealed probe station system using a high resolution parameter analyzer (Agilent B1500A) in the dark to eliminate water moisture and environmental effects.

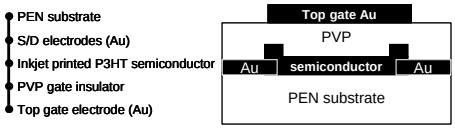

Fig. 1 Process flow and device structure of studied OTFTs.

To clarify stress temperature, gate bias, and time effects individually on OTFTs, we performed *I-V* characterization at temperature ranging from 300 to 370 K before bias stress measurement. Figure 2 plots the temperature-dependent transfer characteristics at V_{ds} = -40 V and the corresponding V_{th} and *SS*. V_{th} is determined by a constant current criteria of I_d/W = 0.1 μA/μm and I_{on} is the drain current at $V_g - V_{th}$ = -30 V. If the organic materials P3HT and PVP are thermally stable in the temperature regime, intuitively V_{th} would shift positively with temperature in company with *SS* degradation for enhanced thermal-activated carriers. In addition, increasing temperature is expected to reduce I_{on} and increase I_{off} for enhanced phonon scattering and degraded junction leakage, respectively. However, our experimental data show reverse temperature-dependent subthreshold behaviors in Fig. 2(b) and (c). There are three temperature zones: in zone-I (300-320 K), the fact of negative V_{th} shift (ΔV_{th}) and *SS* reduction with temperature is opposite to aforementioned prediction, and such temperature-dependent V_{th} and *SS* behaviors become more manifest in zone-II (320-350K). Interestingly *SS* is proportional to

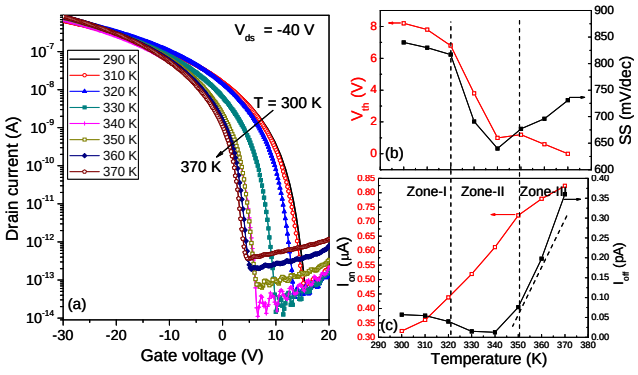

Fig. 2 Temperature-dependent (a) transfer curves, (b) V_{th} and *SS*, and (c) I_{on} and I_{off} of studied OTFTs.

temperature ($SS \propto k_BT$) and the V_{th} decline is suppressed as temperature increases to 350 K or higher in zone-III. Notably the dependence of I_{on} and I_{off} on temperature acts in concert with that of *SS*. The significant I_{on} enhancement at high temperature is the benefit of a considerable *SS* reduction. The unanticipated *SS* and I_{on} improvement at high temperature indicates that the effectiveness of eliminating interface traps or expelling water moisture by high temperature anneal outperforms the phonon scattering effect on charge transport. This is further evidenced by I_{off} reduction with temperature in zone I and II. Most importantly, a systematic negative V_{th} shift with temperature is a strong indicative of positive charges generation within PVP insulator, dopant deactivation or bipolaron formation [4] in P3HT semiconductor with increasing temperature.

To suppress water moisture effects, samples were annealed at 370 K for 30 min before stress measurements. We performed positive (+17 V) and negative (-30 V) gate bias stress tests in order to get further insight into the bias-temperature stress behaviors. Fig. 3(a) shows that a negative gate bias stress causes a monotonic negative ΔV_{th} with stress time for temperature up to 330 K, while *SS* remains nearly unchanged. This is an indicative of positive charge trapping in PVP [2]. Notably a reverse V_{th} motion with stress time appears at t > 60 sec and even a positive ΔV_{th} is obtained as stress temperature reaches 340 K. A maximum positive ΔV_{th} of +4.2 V is observed as stress time reaches to a turning point of 5000 sec, and then V_{th} shifts back negatively again for longer stress time. Such a reversible ΔV_{th} behavior is observable but suppressed at higher stress temperature. For reference, ΔV_{th} with stress time without gate bias stress at 370 K is also plotted to assess the gate bias stress effect on V_{th} instability. It is clear to see that the V_{th} instability is accelerated by bias stress and the reversible ΔV_{th} is mainly conducted by bias stress. Remarkably bias stress induced ΔV_{th} could be almost recovered by a post-stress anneal at 370 K for 30 min, as shown in Fig. 3(c). It is noted that a positive ΔV_{th} is observable only at T = 330-350 K, corresponding to the zone II of Fig. 2 in which a significant SS reduction and a negative V_{th} shift occur. If we subtracted the ΔV_{th} hump from corresponding curves in Fig. 3, time-evolutional ΔV_{th} could be described by a stretched-exponential decay equation of $|\Delta V_{th}| = V_0\{1-\exp\{-(t/\tau)^{\beta}\}\}$, where V_0 is the applied gate bias, τ is the characteristic trapping time of carries and β is the dispersion parameter. The extracted characteristic trapping time and dispersion parameter are plotted in Fig. 3(d), in which we cannot obtain a straight line either for τ or β. This indicates that charge trapping is not a sole origin for V_{th} instability. τ and β become stress temperature independent with a value of 2.35×10^6 sec and 0.33, respectively, at T = 320-350 K, in which a positive ΔV_{th} appears in Fig. 3(b) as well. It is noted that a positive gate bias stress also produces a predominately negative ΔV_{th} with stress time and temperature, except a positive ΔV_{th} for conditions of T = 310-330K and stress time > 1000 sec in Fig. 4. A possible explanation has been proposed for positive ΔV_{th}, and water absorption induced negative ions drift in the gate field may be its origin. However, this could not explain well our experimental observations, in particular, the V_{th}, *SS*, and reversible ΔV_{th} behaviors at T = 320-350 K. We suggest that, in addition to thermally activated charge trapping and ion drift mechanisms, the trap numbers elimination at the P3HT/PVP and the dopant deactivation or bipolaron formation in P3HT are also possible origin for OTFTs instability.

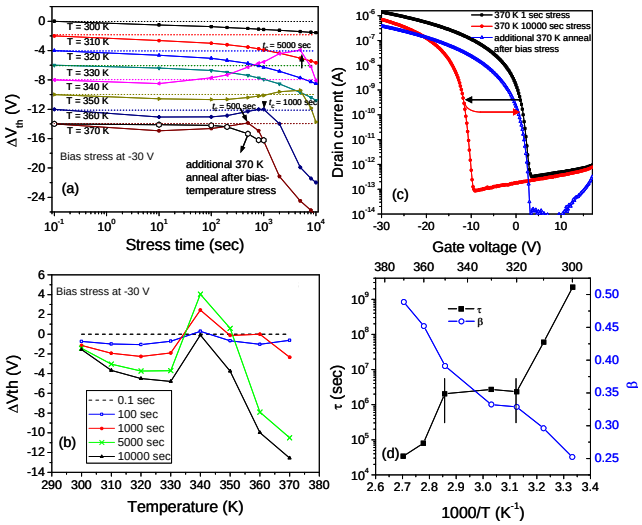

Fig. 3 (a) and (b) V_{th} shift as functions of stress time and stress temperatures at a negative gate bias of -30 V. Curves in (a) were vertically shifted by -2 V sequentially for clarity. (c) transfer characteristics of OTFTs after bias-temperature stress and additional post-stress anneal at 370 K. (d) extracted relaxation time and stretched-exponential dispersion parameter as a function of reciprocal temperature.

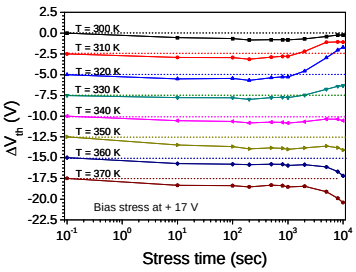

Fig. 4 ΔV_{th} as a function of stress time and stress temperatures for a positive gate bias of +17 V. Curves were vertically shifted by -2.5 V sequentially for clarity.

Acknowledgements

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References

[1] S. J. Zilker, C. Detcheverry, E. Cantatore, and D. m. de Leeuw, Appl. Phys. Lett., **79** (2001) 1124.

[2] S. G. Mathijssen, M. Colle, H. Gomes, E. C. Smits, B. de Boer, I. McCulloch, P. A. Bobbert, and D. M. de Leeuw, Adv. Mater. 19 (2007) 2785.

[3] H. L. Gomes, P. Stallinga, F. Dinelli, M. Murgia, F. Biscarini, D. M. De Leeuw, T. Muck, J. Geurts, and L. W. Molenkamp, Appl. Phys. Lett., **84** (2004) 3184.

[4] A. Salleo and R. A, Street, Phy. Rev. B, **70** (2004) 235324.