Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp956-957

Transport Mechanism at the First-layered Pentacene Grains and Grain Boundaries

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1. Introduction

Charge transport in organic thin-film transistors (OTFTs) is being widely studied because of their potential applications in flexible organic elelctronics.[1, 2].One main scientific challenge is to clarify the transport mechanism in the polycrystalline organic films and to establish the relationship between the film structure and the device performance. Charge transport in OTFTs has been demonstrated to occur just in a few layers at the interface of active layers and dielectrics.[3, 4] Therefore, it is more reasonable to relate the mobility with film structure using the grain sizes at the first layer of semiconductor films.

In this work, pentacene thin-film transistors have been fabricated on various dielectrics and thus realized the different grain sizes at the first layer of the films and accordingly different mobility of the transistors. It is found that the mobility does relate with the first layer grain sizes and this relationship could be explained by a grain boundary model. In addition, the temperature dependent mobility experiment was carried out and the results also accord well with the grain boundary model.

2. Experiment

Heavily *n*-doped Si wafers with thermally grown oxide layer of 250 nm were utilized as the substrates (gate electrode). polymethyl methacrylate (PMMA), polycarbonate (PC) and polystyrene (PS) were spin-coated onto the substrates to form the bi-layer dielectrics, respectively.[5] 50nm pentacene (Aldrich Co.) films were deposited through thermal evaporation (Auto-306 BOC-Edwards Co.) under a vacuum pressure of 7×10^{-5} Pa with a deposition rate of 0.02nm/s on four dielectrics in the same growth run. 50nm Au films deposited onto the pentacene form the source and drain electrode with a channel length L=50 μm and width W=2000 μm. To investigate the grain sizes at the first layer of the pentacene films, 1nm pentacene (about 2/3 monolayer) were deposited onto the various dielectrics under the same conditions.The electrical characteristics of the transistors were measured with a Keithley 4200 semiconductor analyzer.

The devices fabricated on PC/SiO_2 were also measured in a TTP4 Probe Station (Lake Shore Cryotronics, Inc.) under vacuum conditions for a variant temperature experiment.The surface morphologies of the 1nm and 50nm pentacene films were characterized by a Nanoscope III (Vecco Co.) atomic force microscopy (AFM).

3. Results and discussion

a. Correlation between mobility and grain sizes

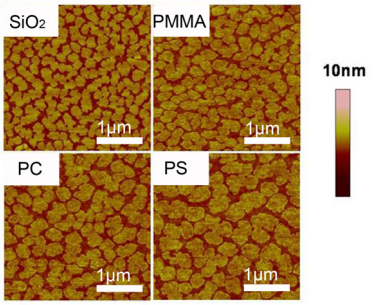

Fig. 1 3 ×3 μm^2 AFM images of 1 nm thick pentacene films deposited on four different dielectrics.

As shown in **Fig. 1**, the 1nm pentacene films deposited on different dielectrics exhibit different grain sizes, and accordingly, the mobility of transistors deposited on these dielectrics are different. The grain sizes at the first monolayer were extracted from the initial nucleation densities shown in **Fig. 1** by assuming that the further growth of extra pentacene molecules would heal the gaps among the existed grains before one complete monolayer formed. **Fig. 2(a)** shows that the mobility of transistors increases with the increasing grain sizes at the first layer, which indicates that the mobility is determined by the grain sizes at the first layer of the films.

In order to clarify the correlation between mobility and grain sizes at the first layer, some simulation based on the grain boundary model were carried out. This model simply assumes that the organic films consist of grains of average length L_G and mobility μ_G connected with grain boundaries of average length L_{GB} and mobility μ_{GB}. **Fig. 2(b)** shows the diagram of the model. The effective mobility is then given as[6]:

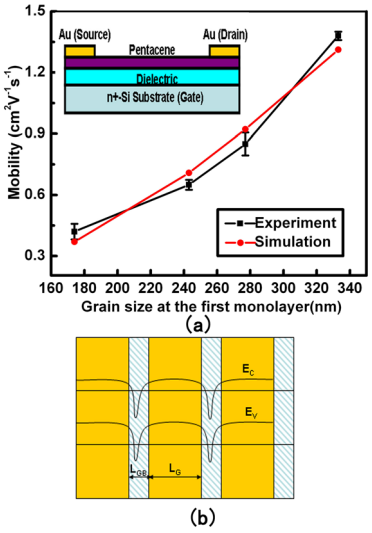

Fig. 2(a)The schematic diagram of OTFTs (inset) and experiment (square) and simulation (circle) results of the mobility as a function of grain sizes at the first layer under V_{DS}=-40V in ambient condition. (b) The diagram of the grain boundary model and its energy diagram.

$$\mu_{eff} = \frac{\mu_G}{1 + \frac{\mu_G}{\mu_{GB}} e^{qV_b/kT} \frac{L_{GB}}{L_G + L_{GB}}} \qquad (1)$$

where $E_b = qV_b$ is the grain boundary barrier height. **Fig. 2(a)** shows the fitting result, which fits well with the experiment data and yields reasonable values of μ_G =26.76 cm^2/Vs, L_{GB} =1.48 nm, and $e^{qV_b/kT} / \mu_{GB}$ =164.17.[7]

b. Temperature dependent transport properties

The temperature dependent transport properties of transistors deposited on the PC/SiO_2 dielectric were systematically investigated and the carrier mobility at different temperatures was extracted from the transfer characteristics shown in **Fig. 3.** Simulations carried out with Eq. (1) using μ_G=26.76 cm^2/Vs, L_{GB} =1.48nm fit with the experiment. Moreover, μ_{GB} =0.013cm^2/Vs and qV_b =19.2 meV was given by the simulation, and accordingly, $e^{qV_b/kT} / \mu_{GB}$ =161.53, which compares well with the result of the grain size dependent mobility.

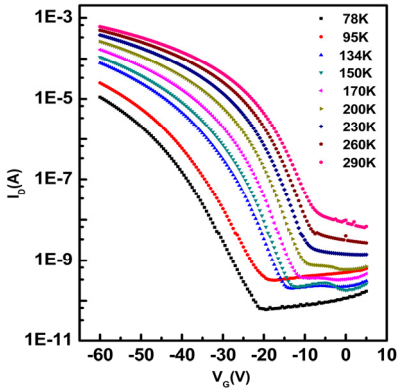

Fig. 3 Transfer characteristics of the transistors using the PC/SiO_2 dielectric at various temperatures.

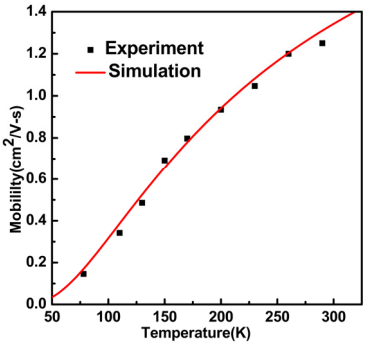

Fig. 4 Comparison of experiment (square) and simulated field-effect mobility vs temperature for the petacene thin-film transistors deposited on the PS/SiO_2 dielectric in vacuum condition.

4. Conclusions

We have performed both the experimental and theoretical researches of transport mechanism in the first layer grains and grain boundaries of the pentacene films. It is found that the grain boundary model is valid in the grain size dependent mobility experiment as well as in the temperature dependent mobility experiment.

References:

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