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Realization of Pentacene-based Thin Film Transistor Arrays for Large-area Organic Electronics Being Compatible with the Roll-to-Roll Manufacturing Technique

Liangmin Wang, [1, 2] Dexing Li, [1] and Chao Jiang, [1, a)]

National Center for Nanoscience and Technology, 11 Beiyitiao Zhongguancun, Beijing 100190, China

[2]Graduate School of Chinese Academy of Sciences, Beijing 100049, China

[a)] Phone: +86-10-8254-5563 E-mail: jiangch@nanoctr.cn

Introduction

Organic electronic devices show inherent advantages of simple fabrication process, low cost, compatibility with flexible substrate, near room temperature fabrication and the potential for large-scale mass production, and therefore are promising to be widely used in next generation electronic devices and integrated circuits [1]. Organic thin film transistors (OTFTs) will only be able to achieve their low cost potential if they can be processed with a high throughput, e.g., in a roll-to-roll or sheet-to-sheet production on foil. One of the many successive processing steps in the production is the deposition of the organic semiconductor. The selected technique should deposit thin films at a high speed over large substrates with a well-controlled morphology, high uniformity and good reproducibility of the electrical characteristics. In this work a vacuum thermal evaporation (VTE) is extended to a VTE-roller method that may be compatible with a roll-to-roll manufacturing technique. We show that the technique combines high uniformity with excellent performance of the deposited arrays of OTFTs on large areas.

VTE roller system

Figure 1 shows the schematics of the home-made VTE roller system. A cylindrical roller used as sample set locates in the center of the deposition chamber. The roller reciprocally moves along horizontal axis at a speed from 1 mm/s to 15 mm/s and rotates around the axis at a speed from 20 mm/s to 220 mm/s (line speed), simultaneously. The outer surface of the roller 160mm in diameter allows mounting a flexible substrate with dimension up to 300 mm × 500 mm^2. In principle, this design can be extended to deposition on a larger sheet or roll. The motors are placed outside to keep high vacuum in the deposition chamber and the power is transferred by a magnetic flux connection. Two conventional furnaces (k-cells) for organic semiconductors and an evaporation source for metals locate at the bottom of the deposition chamber. Several quartz oscillators are placed over the evaporation source to real-time monitor the film growth rate. The deposition chamber is equipped with a loadlock on the other side, allowing for fast loading and unloading of the samples.

Experimental

Top-contact pentacene thin film transistors (TFTs) are fabricated on two kinds of substrates. One is highly doped n^{++} silicon wafer (15×15 mm^2), and the other is polyethylene terephthalate foil with indium tin oxide coating (PET-ITO, 80×80 mm^2) which used as gate electrode. Polystyrene (PS) (molecular weight = 100 000) was dissolved in toluene with a concentration of 5 wt %, then was spin coated onto the substrates and crosslinked at 85 °C for 8 h in a vacuum oven with a final thickness of 425 nm. Pentacene (purity 97% from Aldrich Co.) films with thickness of 35 nm were grown onto PS by utilizing the VTE roller system. During pentacene deposition, the chamber pressure was 6×10^{-5} Pa and the furnace temperature was set for guaranteeing the deposition rate similar to the conventional evaporation system. In the VTE roller system, the roller translational speed was 10 mm/s and the rotational speed was 150 mm/s. After pentacene deposition, 40 nm-thick Cu or Au source-drain electrodes were deposited onto the pentacene layer through a flexible metal shadow mask in the VTE roller system. The channel length was 50 μm on Si substrate and 100 μm on PET substrates, and the channel widths were both 2000 μm.

The morphology of the pentacene film was characterized by atomic force microscope (AFM) with NanoScope III (Veeco Co.) using tapping mode. The film thickness is systematically measured post growth using daktak-150 surface profiler (Veeco Co.). The current-voltage characteristics of the TFTs were measured by a Kethley-4200 semiconductor analyzer in ambient.

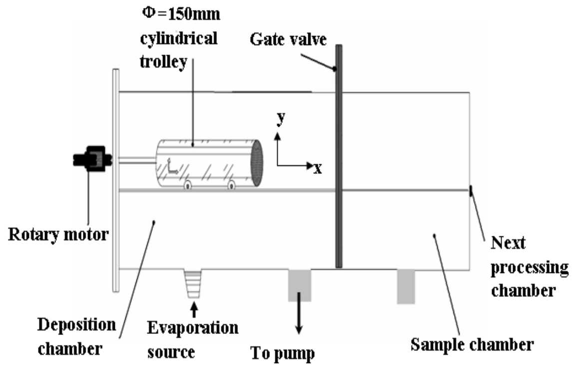

Fig. 1 Schematics of the VTE roller system used in this work.

Results and discussion

Figure 2(a) shows the morphology of 35 nm pentacene film grown on PS dielectric by this VTE roller system. For comparison, pentacene film was also deposited using a commercial thermal evaporator Auto-306 (BOC-Edwards Co.). The pentacene grains exhibit similar dendritic terraced structure in these two deposition systems, however with little different grain sizes as shown in Fig. 2. The factors affecting the grain size include substrate temperature, surface clean method, and deposition rate. The latter one is the main factor in the different grain size between the two deposition systems.

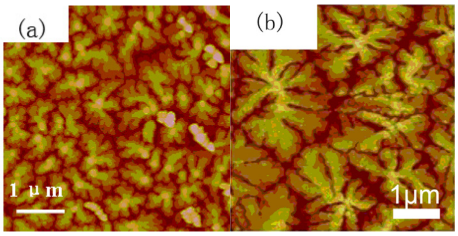

Fig. 2 AFM images of 50 nm thick pentacene deposited on PS in (a) the VTE roller system with a deposition rate of 1500 nm·cm^2/min and (b) a commercial thermal evaporator Auto-306 with a deposition rate of 0.02 nm/s.

In the VTE roller system, the growth speed, R_S, with unit of nm·cm^2/min, can be expressed by

$R_S = d \times A/t$, where d, A, t is the final film thickness, the substrate area and the deposition time, respectively. The area of the VTE roller system is 300×500 mm^2, equal to 1500 cm^2. 1500 nm·cm^2/min deposition rate in VTE roller system corresponds to about 0.12 nm/s in Auto-306.

Figure 3 shows the thickness distribution of pentacene film grown over a 300×500 mm^2 sheet in the VTE roller system. The average thickness is 85±5 nm and the standard deviation over the whole sheet is 2.7%. The calibration was carried out based on 42 positions which uniform distributed in the 300×500 mm^2 sheet. This low standard deviation represents the VTE roller system has a high film deposition uniformity.

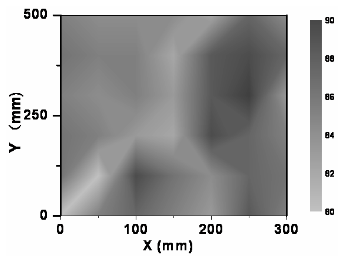

Fig. 3 Thickness map of a typical pentacene film over a 300×500 mm^2 PET-ITO sheet.

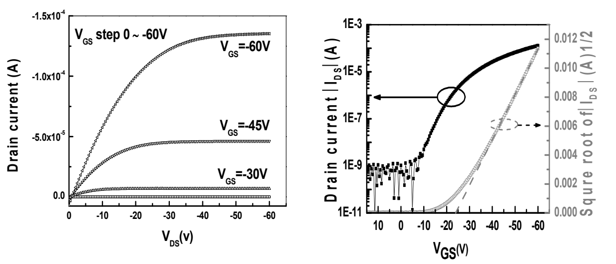

Fig. 4 Typical output curves (V_{DS}=-60V) and transfer curves of pentacene TFTs prepared on Si substrates.

Figure 4 represents the typical transfer curves and output curves of pentacene TFTs prepared on 42 Si substrates (on 42 calibration sites), which were stick uniformly onto the roller. Pentacene TFTs characteristics are apparently well behaved. The average mobility, extracted in saturation region, is 0.88±0.12 cm^2/Vs. The standard deviation of the mobility over 300×500 mm^2 is 10%. The average threshold voltage is -24.7V with standard deviation of 10%. The on/off ratio is more than 1×10^5.

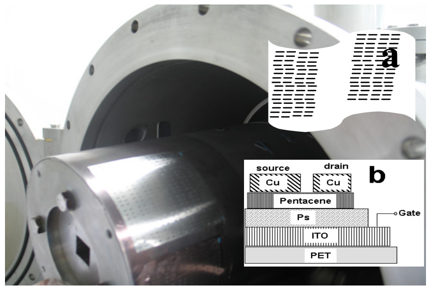

Fig. 5 Photograph of the roller VTE. The inset a: Schematics of the pentacene TFT arrays on PET sheet; the inset b: the structure of the TFT.

Figure 5(a) represents the Schematics of the pentacene TFT arrays on PET-ITO (80×80 mm) sheet. Pentacene TFTs also shows favorable electrical performance and high uniformity. The average mobility extracted in saturation region based on 20 uniformly distributed devices is 0.34±0.04 cm^2/Vs with the standard deviation of 10%. The on/off ratio is from 1×10^4 to 2×10^4. Although OTFT device performance has deteriorated as flexible PET-ITO substrates instead of highly doped silicon, the device performance uniformity within large area is still guaranteed.

In addition, the continuous operation for several months demonstrated the robustness of the VTE roller system very well. The electrical properties of the pentacene TFTs is almost unchanged if we systematically change the evaporation rate from 900 nm·cm^2/min to 1500 nm·cm^2/min and the rotation speed from 100 mm/s to 200 mm/s.

Conclusions

A VTE roller system has been developed and optimized for deposition of uniform pentacene thin films on large area. Electrical characterization of arrays of pentacene TFTs has been carried out through measurements of top-contact thin film transistors. The film thickness and device performance show high uniformity for the arrays of OTFTs with standard deviation less than 10% and good reproducibility. The saturation mobilities have met the device demonstration requirements. The VTE roller system is a very promising candidate for the roll-to-roll processing of small molecular weight organic semiconductors.

References

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